DESIGN OF A HIGH EFFICIENCY CLASS-F POWER AMPLIFIER INTEGRATED WITH A MICROSTRIP PATCH ANTENNA

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ABSTRACT

This thesis presents the research carried out into the effects of load and source harmonic terminations on the efficiency of a class-F power amplifier (PA). A demonstration on the direct integration of the class-F PA and an H-shaped patch antenna using an active integrated antenna (AIA) approach is also presented.

To obtain a high efficiency PA, it is necessary to ensure that the power dissipated in the active device is minimised and this is achieved by ensuring that the overlapping area between the drain voltage and current waveforms in the time domain is minimised. To minimise this overlapping area, optimum source and load harmonic impedances for the fundamental frequency, and second and third harmonics, are obtained using a novel application of the simulated load/source-pull method.

New forms of harmonic matching networks were designed to ensure that the active device is terminated by the optimum impedances at the gate and drain for maximum efficiency. Three PAs were designed, one operating at 0.9 GHz and the other two at 2.45 GHz. For the 0.9 GHz PA the load matching network was designed to obtain the required optimum impedances at the fundamental frequency, and second and third harmonics. As the effect of gate capacitance is small at this frequency, the source matching network was designed to obtain a conjugate match at the fundamental frequency only. At the higher frequency of 2.45 GHz, the gate capacitance has a larger effect on the efficiency of the PA and hence two designs were investigated and compared. In the first PA design the load and source matching networks were designed to obtain optimum impedances at the fundamental frequency and second harmonic. For the second PA design, these networks were designed to obtain optimum impedances at the fundamental frequency, and second and third harmonics. For these three PAs the simulated drain voltage/current waveforms, return loss, stability factor, power gain, output power and power added efficiency (PAE) are presented. The practical results are compared with those obtained by

simulation. Each PA produced a PAE of greater than 70% and good agreement was obtained between the simulated and measured results. The PAE obtained in these works is comparable to that reported in published papers. Based on this research five papers have been published in journals and conferences.

An H-shaped microstrip patch antenna is used in the active integrated antenna (AIA) design. The antenna must not only act as a radiator and a harmonic suppresser but also as an optimum load for the PA so that it can be connected directly to the active device in order to obtain maximum efficiency. An extensive study on this antenna was carried out. The formulas for the first four mode frequencies were derived using odd and even mode analysis while a new and simpler formula for the fourth mode frequency was obtained. A systematic design approach to obtain the dimensions of the antenna is presented for an antenna operating at a given fundamental mode frequency. For matching, a new explicit matrix input impedance formula for the H-shaped antenna has been obtained using segmentation method. Using this formula, the location of the probe feed could be adjusted to obtain the required impedance at the pre-assigned frequency. MathCAD programming is used to implement the calculations in the design of two antennas. Good agreement between the predicted, simulated and measured results is obtained for the resonant mode frequencies, input impedance and return loss. Based on this research two papers have been published in journals.

Two AIA designs operating at 2.45 GHz are presented in this thesis. In the first design the load and source matching networks used in the PA were employed with the H-shaped antenna replacing the 50 Ω load. In order to further minimise the size, cost, and losses, a new second AIA design was proposed. A probe feed location was found to obtain the required optimum impedance at the fundamental frequency, and, the drain bias network was used to obtain the required optimum impedance at the second harmonic. For both designs the simulated drain voltage/current waveforms, return loss, stability factor, PAE,

output power and power gain were obtained. The two AIAs were fabricated and the practical results obtained were found to be in good agreement with those obtained by simulation. These AIAs achieved a measured PAE of more than 67% and also good harmonic suppression at the higher harmonics. Again, the PAE obtained in these designs is comparable to the results reported in published papers. All the simulations were carried out using Agilent's Advanced Design System (ADS) software tool.

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DECLARATION

I declare that the work contained in this thesis has not been submitted for any other award and that it is all my own work.

Name: Shirt Fun Ooi

Signature:

Date: 20 August 2007

GLOSSARY OF ACRONYMS

PA	.....	Power amplifier
AIA	.....	Active integrated antenna
PCB	.....	Printed circuit board
PAE	.....	Power added efficiency
GSM	.....	Global system for mobile communications
WLAN	.....	Wireless local area network
ADS	.....	Advanced design system
CAD	.....	Computer-aided design
DC	.....	Direct current
AC	.....	Alternating current
RF	.....	Radio Frequency
FET	.....	Field effect transistor
GHz	.....	Gigahertz
Ge	.....	Germanium
Si	.....	Silicon
BJT	.....	Bipolar junction transistor
GaAs	.....	Gallium arsenide
MESFET	.....	Metal-semiconductor field effect transistor
HBT	.....	Heterojunction bipolar transistor
HFET	.....	Heterojunction field effect transistor
HEMT	.....	High electron-mobility transistor
pHEMT	.....	Pseudomorphic high electron-mobility transistor
InP	.....	Indium phosphide
AlGaAs	.....	Aluminium gallium arsenide
InGaAs	.....	Indium gallium arsenide

GaN	.....	Gallium nitride
SiC	.....	Silicon carbide
LF	.....	Low frequency (30 kHz to 300 kHz)
MF	.....	Medium frequency (300 kHz to 3000 kHz)
HF	.....	High frequency (3 MHz to 30 MHz)
VHF	.....	Very high frequency (30 MHz to 300 MHz)
UHF	.....	Ultra high frequency (300 MHz to 3 GHz)
AM	.....	Amplitude modulation
HP	.....	Harmonic-peaking
HB	.....	Harmonic balance
LSSP	.....	Large signal S-parameters
DUT	.....	Device-under-test
PCS	.....	Personal communications systems
LNA	.....	Low noise amplifier
TM	.....	Transverse magnetic
FDTD	.....	Finite difference time domain
PBG	.....	Photonic band gap
PIFA	.....	Planar inverted-F antenna
EM	.....	Electromagnetic
MoM	.....	Method of moments

GLOSSARY OF SYMBOLS

η_d	.....	Drain efficiency
P_{out}	.....	AC output power
G_p	.....	Power gain
P_{in}	.....	AC input power
P_{dc}	.....	DC power supplied
P_{diss}	.....	Power dissipated
η_{av}	.....	Average efficiency
R_L	.....	Load resistance
I_{max}	.....	Maximum current
I_{dss}	.....	Total device drain current
I_{ds}	.....	Drain current
V_{gs}	.....	Gate voltage
V_{ds}	.....	Drain voltage
V_{dd}	.....	Drain bias voltage
V_{gg}	.....	Gate bias voltage
V_p	.....	Pinch-off voltage
V_q	.....	Quiescent voltage
I_q	.....	Quiescent current
I_{dc}	.....	DC component of the drain current
V_{out}	.....	Output voltage
C_{ds}	.....	Drain capacitance
C_{gs}	.....	Gate capacitance
C_{gd}	.....	Gate-drain capacitance
R_{ds}	.....	Drain-source resistance (Output resistance)
R_i	.....	Gate charging resistance

L_d	.....	Drain bonding lead inductance
L_g	.....	Gate bonding lead inductance
L_s	.....	Source bonding lead inductance
R_d	.....	Drain bonding lead resistance
R_g	.....	Gate bonding lead resistance
R_s	.....	Source bonding lead resistance
C_{pg}	.....	Pad capacitance at gate
C_{pd}	.....	Pad capacitance at drain
I_n	.....	N^{th} component of the drain current
V_n	.....	N^{th} component of the drain voltage
ξ_n	.....	Phase of the n^{th} harmonic component of the drain current
ψ_n	.....	Phase of the n^{th} harmonic component of the drain voltage
$Z_{ds,nf}$	.....	Impedance across the drain to source device terminals
V_k	.....	Knee voltage
g_m	.....	Transconductance
P_R	.....	Reflected power
Z_S	.....	Source impedance
Z_L	.....	Load impedance
λ	.....	Wavelength
f_1	.....	Fundamental frequency
Z_0	.....	Characteristic impedance
θ	.....	Electrical length
C_{block}	.....	DC block capacitor
Z_{in}	.....	Input impedance
h	.....	Thickness
L	.....	Length

W	.....	Width
Y	.....	Admittance
$\bar{E}$	.....	Electric field
$\bar{H}$	.....	Magnetic field
α	.....	Attenuation constant
γ	.....	propagation constant
ε_0	.....	Permittivity of free space (=8.854 x 10^{-12} F/m)
ε_r	.....	Relative permittivity of dielectric or dielectric constant
ε_{reff}	.....	Effective permittivity of dielectric or effective dielectric constant
ϕ	.....	Eigenfunctions of patch antenna
η_0	.....	Impedance of free space (=376.7 Ω)
λ_0	.....	Free-space wavelength
μ	.....	Permeability of dielectric
μ_0	.....	Permeability of free space (=4π x 10^{-7} H/m)
μ_r	.....	Relative permeability of dielectric
σ_c	.....	Conductivity of conductor
ω	.....	Angular frequency
ΔL	.....	Line extension due to fringing fields
B_1	.....	Capacitive susceptances due to fringing fields
c_0	.....	Speed of light in free space (2.998x10^8 m/s)
G_1	.....	Radiation conductance
G_{12}	.....	Mutual conductance
J_0	.....	The order zero Bessel function of the first kind
k_0	.....	Phase constant in free space ($=2\pi/\lambda_0$)

$k_{m,n}$	.....	Wavenumber of TM_{mn} modes in dielectric
$\tan\delta$	.....	Dielectric loss tangent
Y_c	.....	Characteristic admittance
G	.....	Green's function
J	.....	Current density
f	.....	Frequency
dB	.....	Decibel

SUBSTRATE AND ITS PARAMETERS

The substrate and its parameters used in this thesis

RT Duroid 5870

Substrate's thicknesses: h = 0.79 mm and h = 1.575 mm

Dielectric loss tangent: tan δ=0.0012

Dielectric constant: ϵ_r=2.33

CHAPTER 1 INTRODUCTION AND OVERVIEW OF THESIS

1.1 Introduction

Efficiency, size and cost are important requirements for a transmitter front-end used in mobile wireless and satellite communication systems [1]. To reduce battery power consumption in the transmitter it is important to minimise the power loss in the PA and hence recent research has focused on the different approaches used to increase the dc to ac power conversion. Also, by reducing the size of the transmitter it is possible to obtain smaller handheld devices or add additional features to the system. The research into size reduction has concentrated on the AIA design approach [2], [3]. The areas of research carried out in this thesis are the design of a high efficiency PA and a compact harmonic suppressed antenna. The thesis also addresses the problem of direct integration of the antenna and the PA so that the size of the transmitter can be further reduced. These research areas are reviewed below.

The efficiency of the PA is increased if the overlapping area between the current and voltage waveforms at the output of the active device is reduced. This reduction in the overlap is obtained by switching the active device 'on' and 'off' and is used in the designs of high efficiency PAs [4], [5]. In these designs the active device is driven by a large input signal and hence it is necessary to use nonlinear modelling of FET. Different nonlinear models and analyses of the FETs are reviewed in the thesis. Based on the Statz model [6], a novel application of the simulated load/source-pull method is used to determine the required optimum load/source harmonic impedances to obtain maximum efficiency. The simulated gate voltage waveform and the drain voltage/current waveforms are then used to investigate how the efficiency is affected by each of the harmonic impedances. Two new proposed harmonic matching networks were designed to ensure that the active device was

terminated by the optimum impedances at the gate and drain for maximum efficiency. One PA operating at 0.9 GHz and two PAs operating at 2.45 GHz were designed and fabricated.

In the AIA design an H-shaped antenna with a probe feed is used as a radiating element as it is both compact and can be designed for harmonic suppression. First, a systematic design strategy is presented for the antenna using empirical parametric studies and employing a two dimensional contour plot. A new augmentation method is used to reduce the number of coplanar matrix circuit equations to obtain a new explicit matrix input impedance formula. Some of the elements in the matrix are evaluated using a new explicit computationally efficient coupling impedance formula between the probe and a perimeter port, and, a new probe self impedance formula on a rectangular patch.

In more advanced AIA design the antenna acts not only as a radiating element and a harmonic suppresser but also as an optimum load for the PA so that a high efficiency compact design is obtained [7]. To realise this condition of high efficiency the input impedance of the antenna must satisfy the requirements of the PA load impedances not only at the fundamental frequency but also at other harmonic frequencies. The literature review carried has shown that only a few attempts at direct integration of the antenna and the PA without using load harmonic matching network. This is mainly due to the complexity of designing an antenna with optimum input impedances at the first three frequencies which is necessary for high efficiency. In this thesis a new solution is presented to avoid the use of the load harmonic matching network. This is achieved by finding a suitable probe feed position to obtain an optimum load impedance at the fundamental frequency. Also the drain bias network is used to obtain an optimum load impedance at the second harmonic. Two AIA circuits operating at 2.45 GHz were designed and fabricated.

For the PA, antenna, and, AIA designs, the predicted results are compared with measured and simulated results. A good agreement is obtained between the predicted,

simulated and measured results. The overview of the research carried out is presented in the following section.

1.2 Overview of Thesis

Chapter 2 presents a detailed review of the technical advances made in active devices that have and are currently used in PAs. Also a brief review is presented of the efficiency performance of classical (class-A, AB, B and C) and high efficiency (class-D, E and F) PAs. Detailed analysis and design of a class-F PA where it is assumed that the active device is modelled as a lossless switch is reviewed.

For a practical PA, as the active device does not behave as a perfect lossless switch, the design approach of a class-F PA discussed in Chapter 2 cannot be used. Chapter 3 presents a brief review of the dc and ac nonlinear models of an active device and the different methods used to analyse the nonlinear circuits. In particular the Statz model and harmonic balance (HB) method are used in this thesis. The dc characteristics for the field effect transistor (FET) used in this thesis are presented in this chapter. It is also shown that the FET is unstable at lower frequencies. The values of the resistors connected to the gate terminal are determined to ensure that the FET is stable over the required frequency range.

For a nonlinear model of FET, the load/source-pull method is used to obtain the optimum impedances for maximum efficiency. This method is briefly reviewed and a novel application is used to determine the optimum load and source impedances at the fundamental, second and third harmonics for the class-F PA. These impedances are then used in Chapters 4 and 5 to design the load and source harmonic matching networks. The effect on the efficiency of these optimum source and load impedances at a single frequency, and, also over a frequency range is investigated. Based on this research three papers have been published.

A PA is normally driven by a 50 Ω source and the output power is dissipated in a 50 Ω load. Therefore matching networks must be used at the gate and the drain of the FET so that the active device 'sees' the optimum impedances required to obtain maximum efficiency. Chapter 4 first reviews the published work on the different forms of load matching networks and the efficiencies obtained. A new proposed load harmonic matching network is designed to obtain optimum impedances at a fundamental frequency of 0.9 GHz and also at the second and third harmonics. The source matching network is designed to obtain a conjugate match at the fundamental frequency. The designed PA is then modelled using the ADS software tool to determine the PAE, power gain and output power of the PA. The simulated drain voltage/current waveforms show that minimum power is lost in the FET and that maximum efficiency has been obtained. This PA was fabricated and a good agreement obtained between the simulated and practical results. The practical result is also compared with published results. Based on this research two papers have been published.

At the higher frequency of 2.45 GHz, because of the nonlinearity of the gate capacitance both the load and source harmonic matching networks are needed in the PA design. Based on the optimum impedances obtained from Chapter 3 designs of two new proposed load and source harmonic matching networks at 2.45 GHz are presented in Chapter 5. In the first PA design the load and source matching networks produce optimum impedances at a fundamental frequency and at the second harmonic. In the second PA design load and source impedance matching is obtained at a fundamental frequency and at the second and third harmonics. The simulated results for both designs are presented. Finally, the two PAs were fabricated and the practical results obtained were compared with simulated results and published work. Based on this research a paper has been published.

Chapter 6 briefly reviews the basic characteristics, feed methods and the transmission-line model of a microstrip patch antenna. The circuit elements in the

transmission-line model of a rectangular patch antenna are then derived. A brief review of the cavity model and full-wave model is also discussed. Also different approaches to the reduction in antenna size and different approaches to AIA design are discussed. Explicit efficient coupling impedance formulas for the three different possible locations of two perimeter ports on a rectangular patch are given. These impedance formulas are used in Chapter 8 in the calculation of the probe input impedance of an H-shaped antenna.

In Chapter 7 the difference between a previously published result on an efficient interport coupling impedance formula and the new formula derived in this chapter is given. A new explicit computationally efficient self-coupling impedance formula for a probe feed on a rectangular patch, and also for the coupling impedance between the probe and a perimeter port, are derived. The self, or, input impedance formula is verified by simulation and measurement. Based on the results in this chapter, a new probe matrix input impedance formula is obtained for an H-shaped patch antenna (see Chapter 8) which is used in the AIA design presented in Chapter 9. Based on this research a paper has been published.

In Chapter 8 using odd and even mode analysis, formulas for all the four mode frequencies of an H-shaped patch antenna are derived, including a new and simpler formula for the fourth mode frequency. Using empirical parametric studies a design strategy is presented for the design of an antenna operating at a given fundamental mode frequency. In applying the segmentation method for the determination of the input impedance of H-shaped patch antenna with probe feed a new technique has been employed to reduce the number of matrix circuit equations from five to three. The coupling impedance formulas from Chapters 6 and 7 were used to evaluate the elements in the matrix input impedance formula. Two antennas operating at 2.45 GHz were designed and tested. The predicted and simulated values of resonant mode frequencies, input impedance and return loss for the antennas are then compared with the measured results. Based on this research two papers have been published.

Chapter 9 presents a literature survey of the different design approaches for the AIA circuits. In this chapter two design approaches are used for the AIA circuits operating at 2.45 GHz. In the first circuit the H-shaped antenna was designed so as not to radiate at the second and third harmonics, and, a probe feed position was found so that the input impedance of the antenna was 50 Ω at the operating frequency. This allowed the 50 Ω load of the PA circuit to be replaced by the antenna. Simulated results for the power gain, output power and PAE were obtained for the designed AIA which was fabricated and the practical and simulated results were compared. To further minimise the size and cost the antenna was connected directly to the drain terminal of the FET. To achieve direct integration a probe feed location was found so that an optimum impedance at the fundamental frequency was obtained. The drain bias network was used to obtain the required optimum impedance at the second harmonic. As the antenna was connected directly to the FET the load harmonic matching network was not required and hence the losses and manufacturing costs reduced. The simulated and practical results were found to be in good agreement.

Chapter 10 presents the outcomes of the research carried out and a few suggestions for further development of the new proposed works.

1.3 Significant Research Achievements

- A novel application of the simulated load/source-pull method for obtaining optimum load and source impedances for the class-F PA is presented in the thesis.
- New source and load harmonic matching networks have been designed.
- Using odd and even mode conditions four mode frequency formulas for the H-shaped microstrip patch antenna are derived with a new and simpler formula for the fourth mode frequency.

- A systematic design strategy for an H-shaped microstrip patch antenna operating at a given fundamental mode frequency is presented. This strategy employs empirical parametric studies and a two dimensional contour plot.
- New explicit computationally efficient coupling impedance formulas for the probe feed on a rectangular segment are derived and applied in evaluating the input impedance of an H-shaped microstrip patch antenna.
- A new explicit matrix probe feed input impedance formula for the H-shaped microstrip patch antenna is derived using a new technique to reduce the number of coplanar matrix circuit equations.
- A new approach to the direct integration between the antenna and the PA using the probe feed location and bias network is presented.

1.4 Published Work

Thirteen research papers and a research poster in the area of microstrip patch antenna and PA designs have been published in journals and conferences.

1. S. F. Ooi, S. Gao, A. Sambell, D. Smith, and P. Butterworth, "High efficiency class-F power amplifier design," in *9th IEEE High Frequency Postgraduate Student Colloquium*, Sep. 2004, pp. 113-118.

2. S. K. Lee, A. Sambell, E. Korolkiewicz, S. F. Ooi, and Y. Qin, "Design of a circular polarized nearly square microstrip patch antenna with offset feed," in *9th IEEE High Frequency Postgraduate Student Colloquium*, Sep. 2004, pp. 61-66.

3. S. F. Ooi, S. Gao, A. Sambell, D. Smith, and P. Butterworth, "High efficiency class-F power amplifier design technique," *Microwave Journal*, vol. 47, no. 11, pp. 110-122, Nov. 2004.

4. S. K. Lee, A. Sambell, E. Korolkiewicz, S. F. Loh, S. F. Ooi, and Y. Qin, "A design procedure for a circular polarized, nearly square patch antenna," *Microwave Journal*, vol. 48, no. 1, pp. 116-128, Jan. 2005.

5. P. Butterworth, S. Gao, S. F. Ooi, and A. Sambell, "High efficiency class-F power amplifier with broadband performance," *Microwave and Optical Technology Letters*, vol. 44, no. 3, pp. 243-247, Feb. 2005.

6. S. K. Lee, A. Sambell, E. Korolkiewicz, and S. F. Ooi, "Analysis and design of a circular-polarized nearly-square-patch antenna using a cavity model," *Microwave and Optical Technology Letters*, vol. 46, no. 4, pp. 406-410, Aug. 2005.

7. S. Gao, P. Butterworth, S. F. Ooi, and A. Sambell, "Microwave class-F power amplifier design including input harmonic terminations," in *2005 Asia Pacific Microwave Conference*, Dec. 2005, pp. 3360-3363.

8. S. Gao, P. Butterworth, S. F. Ooi, and A. Sambell, "High efficiency power amplifier design including input harmonic termination," *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 2, pp. 81-83, Feb. 2006.

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10. S. K. Lee, S. F. Ooi, E. G. Lim, E. Korolkiewicz, and A. Sambell, "Efficient coupling impedance formulas for the right-angled isosceles triangular patch for use in segmentation analysis," in *Proc. 36th European Microwave Conference 2006*, Sep. 2006, pp. 241-244.

11. S. F. Ooi, S. K. Lee, A. Sambell, E. Korolkiewicz, and P. Butterworth, "Design of a high efficiency power amplifier with input and output harmonic terminations," *Microwave and Optical Technology Letters*, vol. 49, no. 2, pp. 391-395, Feb. 2007.

12. S. F. Ooi, S. K. Lee, A. Sambell, E. Korolkiewicz, and S. Scott, "Design of H-shaped microstrip patch antennas," *Microwave and Optical Technology Letters*, vol. 49, no. 4, pp. 791-795, Apr. 2007.

13. S. F. Ooi, S. K. Lee, A. Sambell, E. Korolkiewicz, and S. Scott, "A new and explicit matrix input impedance formula for the H-Shaped microstrip patch antenna," *Microwave and Optical Technology Letters*, vol. 49, no. 7, pp. 1756-1759, Jul. 2007.

14. S. F. Ooi, S. K. Lee, A. Sambell, E. Korolkiewicz, S. Gao, and P. Butterworth, "Harmonic-suppressed slot-coupled microstrip patch antenna with enhanced bandwidth," *Microwave and Optical Technology Letters*, vol. 49, no. 8, pp. 1827-1829, Aug. 2007.

15. S. K. Lee, S. F. Ooi, E. G. Lim, E. Korolkiewicz, and A. Sambell, "Explicit efficient coupling impedance formulas for the right-angled isosceles triangle and application to a circularly polarised truncated corners square patch antenna," *IET Microwaves Antenna Propagation*, 2007 (accepted for publication).

16. S. F. Ooi, S. K. Lee, A. Sambell, E. Korolkiewicz, and S. Scott, "A new approach to the design of a compact high efficiency active integrated antenna," *Microwave and Optical Technology Letters* (submitted for review).

CHAPTER 2 REVIEW OF RF AND MICROWAVE POWER AMPLIFIERS

2.1 Introduction

RF and microwave PAs are used not only in many wireless communication systems, but also in radar, medical, and RF heating systems. In all these applications, the PAs convert the dc input power obtained from the dc supply into ac output power. Over the years research has concentrated on the performance of the PA in terms of minimising the power dissipated in the active device and maximising the ac output power by using different power amplification techniques. This has resulted in the design of high efficiency PAs.

In Section 2.2 an overview of a wide variety of active power devices is presented. The efficiency and how effective the active device converts the dc power to ac power is discussed in Section 2.3. A review of the design of ideal classical PAs (class-A, AB, B, and C) [4], [5] and their limitations, is discussed in Section 2.4, where their performance in terms of drain efficiency and output power is compared. In Section 2.5 the design of the ideal high efficiency PAs (class-D, E, and F) [4], [5] is discussed in which a drain efficiency of 100% can be obtained. This is achieved by ensuring that the voltage across, and current through the drain of the active device, do not overlap, so that no real power is dissipated. In Section 2.6, the theoretical analysis of an ideal class-F PA is presented. The drain efficiency of class-F PAs with different harmonic combinations are compared and discussed.

2.2 Development of Solid-State Power Devices

In 1948 Bardeen, Brattain, and Shockley [8], [9], from the Bell Laboratory invented the first bipolar transistor which lead to a communications revolution. However, the RF

gain and noise figure performance were too poor for practical application at microwave frequencies. In 1965, the first practical transistor was fabricated using germanium (Ge). The performance of the Ge devices was limited by low bandgap which resulted in high leakage currents and poor thermal performance. In the late 1960s a silicon (Si) bipolar junction transistor (BJT) was introduced which overcame the above problems and replaced the Ge bipolar transistor.

In the early 1970s, there was a rapid progress in the performance of solid-state active devices. This was mainly due to advances in semiconductor materials, and, processing technology, and allowed the solid-state active device to be used at higher frequencies. With the development of the III-V compound semiconductor (e.g., Gallium arsenide (GaAs)) and the projection photomasking technology, a high-performance GaAs Metal-semiconductor field effect transistor (MESFET) with good RF performance up to 17 GHz was developed in 1970 [10].

By the 1980s improved techniques for semiconductor crystal growth such as molecular-beam epitaxy made the practical heterojunctions a reality for device application. Hence, the 1980s and 1990s saw an increase in a variety of new solid-state devices including the heterojunction bipolar transistor (HBT), the heterojunction field effect transistor (HFET), the high electron-mobility transistor (HEMT), and, the Pseudomorphic HEMT. This allows solid-state devices to be used at higher frequencies. For instance the GaAs HBTs become widely used as the power device in mobile communications and in radar applications at the X-band frequencies.

The development of a variety of new semiconductor materials such as InP, AlGaAs, InGaAs, AlGaAs/GaAs, GaInAs/InP, SiGe, further improved the RF performance of solid-state active devices. This allows the use of InP in HBT to further boost charge mobility so that the active devices could be used above 50 GHz. The currently available AlGaAs/GaAs

HBTs are capable of producing several Watts and extend the upper frequency of operation to over 100 GHz. InP-based HEMT devices the use up to 300 GHz has been reported [11].

However, for the above solid-state devices, due to their low breakdown voltage it is not possible to have an output power up to kilo-Watt. Recently, wide bandgap semiconductors (GaN, SiC, AlGaN/GaN) having a high mobility and high breakdown voltage have been able to generate high output power, comparable to that obtained from microwave vacuum tubes. For instance, SiC MESFETs can produce an ac output power of 4.3 watts per millimeter (W/mm) of the gate width at 10 GHz [12] and GaN-based HEMT can produce an ac output power density as high as 30 W/mm at 8 GHz [13]. The RF power capability of the latter devices compares very favorably with the 1-1.5 W/mm RF power available from GaAs MESFETs, or, GaAs-, or InP-based HEMTs.

In summary, today, solid-state active power devices are widely used in PA circuits from UHF to millimetre-wave ranges approaching terahertz frequencies. The most common devices are GaAs MESFETs which are readily available and are used in X-band and Ku-band applications. For applications at higher frequencies, low cost GaAs HEMTs, pseudomorphic HEMTs, HBTs are also readily available. Further, for applications at even higher frequencies, InP HEMTs provide better performance at higher millimetre-wave frequencies. For high output power applications, SiC MESFETs and GaN HEMTs are a promising technology for high power and high voltages operating at high frequencies. However, the cost of these new wide band gap semiconductor materials is high compared with the cost of other semiconductor materials. Also they are not readily available.

The device used in this thesis (ATF34143) is one of the several commercially available low-cost medium power FETs, which is operational up to a few gigahertzes (GHzs). Most of the devices reported above are from research laboratories (home-grown) and are therefore greater in power capability and frequency range compared to the device used in this thesis.

2.3 PA Design Parameters

The most important design parameters of a PA include power added efficiency (PAE), drain efficiency, η_d, output power, P_{out}, and power gain, G_p. The relationship between the parameters, PAE, η_d, P_{out}, and G_p is obtained from the principle of conservation of energy applied to the PAs structure, Figure 2.1.

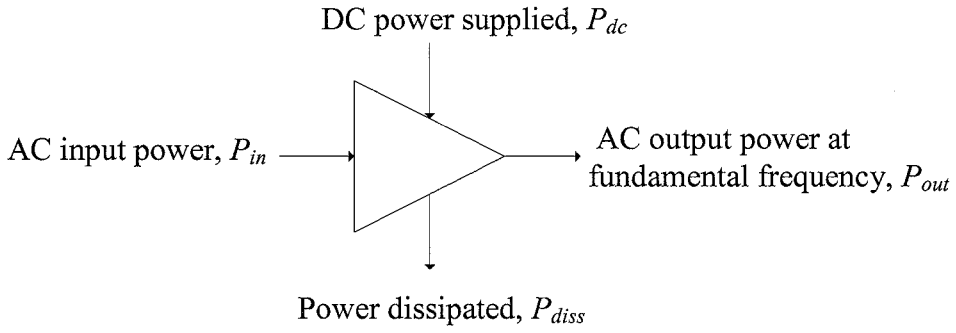


Figure 2.1: PA block diagram.

The total input power must equal the total output power, so that

$$P_{in} + P_{dc} = P_{diss} + P_{out} \tag{2.1}$$

where, P_{in} is the ac input power, P_{dc} is the dc power supplied, P_{out} is the ac output power, and P_{diss} is the total power dissipated in the transistor.

The efficiency of power conversion is called the "PAE", which is defined as,

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \tag{2.2a}$$

Using equation (2.1), it can also be shown that

$$PAE = \frac{P_{dc} - P_{diss}}{P_{dc}} = \eta_d \left[1 - \frac{1}{G_p} \right] \tag{2.2b}$$

$$\text{where, } \eta_d = \frac{P_{out}}{P_{dc}} \tag{2.3}$$

$$\text{and, } G_p = \frac{P_{out}}{P_{in}}. \tag{2.4}$$

Equation (2.2b) shows that the efficiency of dc to ac power conversion depends on the power dissipated in the active device. Hence in order to obtain a maximum PAE, the power dissipated in the active device must be minimised. Minimisation of power dissipation in the active device and the maximising of the output power at the fundamental frequency is the main objective in the design of the high efficiency PAs.

For time varying signals equation (2.3) is modified [14] using average values of, η_d, P_{out}, and P_{dc} over one cycle, so that $\eta_{av}=P_{out\_av}/P_{dc\_av}$.

2.4 Review of Classical PAs

In classical PA designs (class-A, AB, B, and C) it is assumed that the active device operates in the linear region and the output current is not allowed to exceed the saturation point. Also, the active device is considered as an ideal voltage controlled current generator, where the output current is linearly controlled by the input voltage.

Figure 2.2 shows a circuit for the class-A, AB, B, and C PAs.

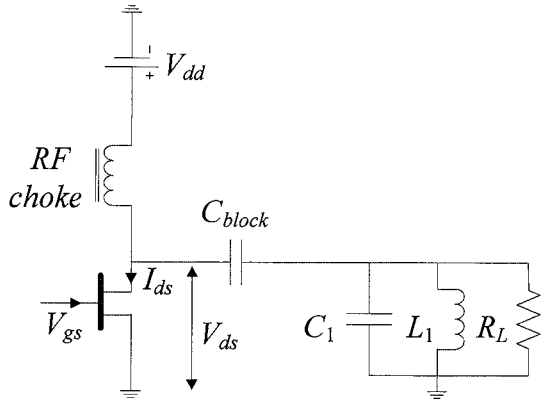


Figure 2.2: Circuit topology for class-A, AB, B, and C PAs.

The dc block capacitor is assumed to be an ideal RF short circuit, and a dc open circuit, while, the RF choke is assumed to be an ideal dc short circuit, and an RF open circuit. For class-AB, B, and C PAs, a tuned circuit (L_1C_1) is used to filter out the higher harmonics,

thus producing a sinusoidal voltage across the load with an amplitude V_{dd}. The load resistance, R_L is set to an optimum value for generating a maximum permissible voltage swing.

For these classes of PAs it is convenient to relate the quiescent bias point, Q, to the conduction angle, α, over the RF cycle when the active device conducts. Figures 2.3, 2.4, 2.5, and 2.6 show the voltage-current relationships for the class-A, AB, B, and C PAs, respectively. I_{max}, I_{dss}, V_{gs}, V_{ds}, V_{dd}, V_p, and I_{ds} are the maximum current, total device drain current, gate voltage, drain voltage, drain bias voltage, pinch-off voltage and drain current. For class-A PA as shown in Figure 2.3, the Q point is located at 0.5 I_{dss}, so that the active device conducts for a full cycle of the input sinusoidal signal v_{gs}, and the conduction angle is 360°.

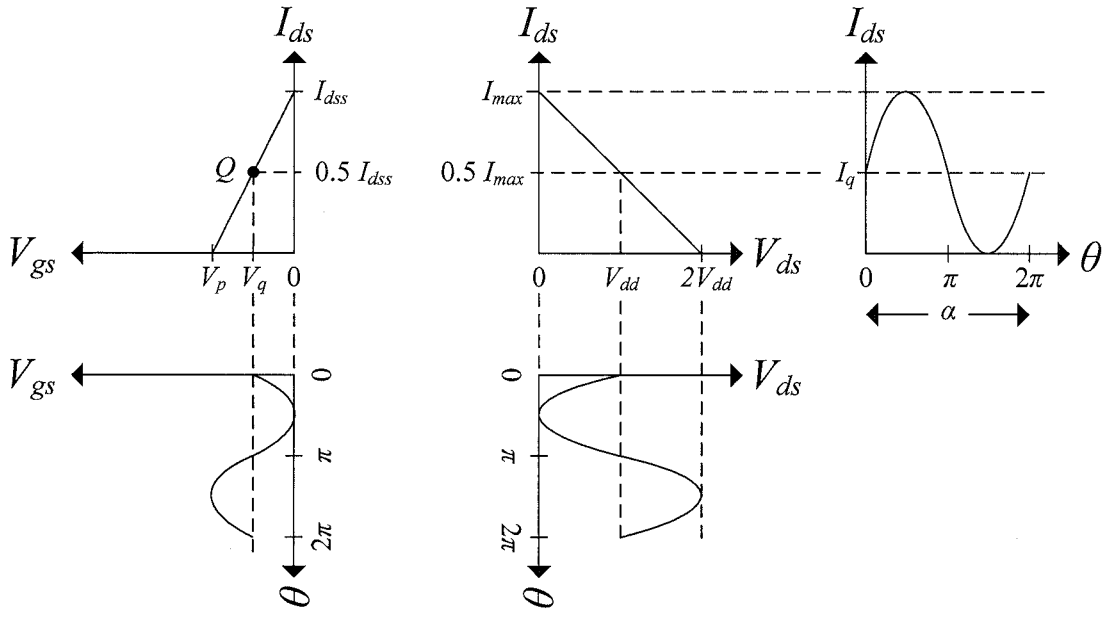


Figure 2.3: Voltage-current relationships for an ideal class-A PA.

For class-AB, B, and C PAs the active device is biased at a Q point beyond 0.5 I_{dss}. For class-AB PA the Q point is chosen so that the conduction angle is in the region $180° < \alpha < 360°$ as shown in Figure 2.4.

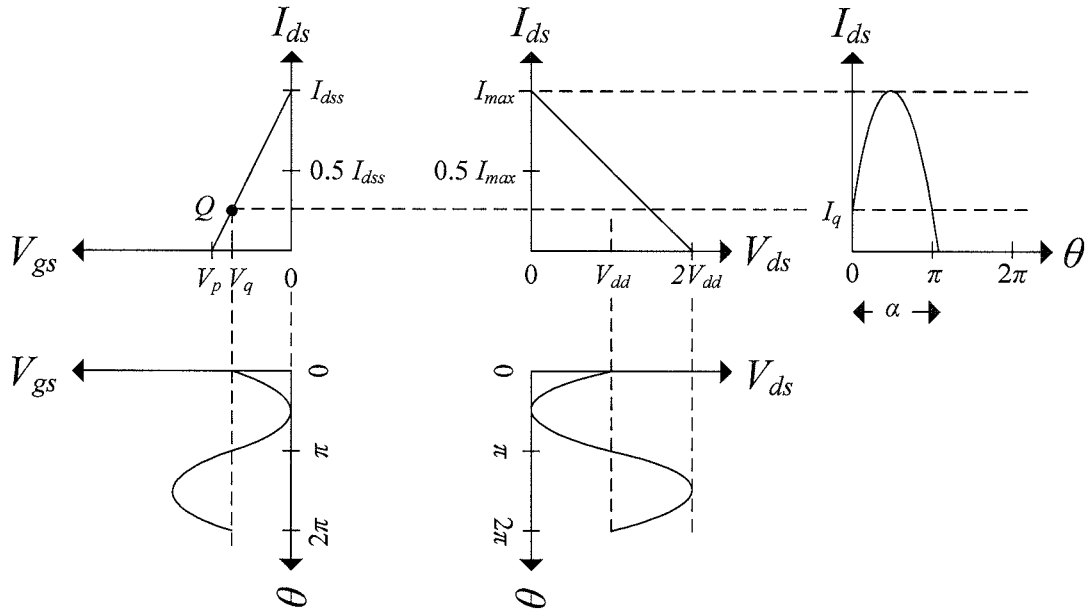


Figure 2.4: Voltage-current relationships for an ideal class-AB PA.

For class-B PA (see Figure 2.5) the Q point is set at the pinch off voltage V_p of the active device so that the conduction angle is 180°.

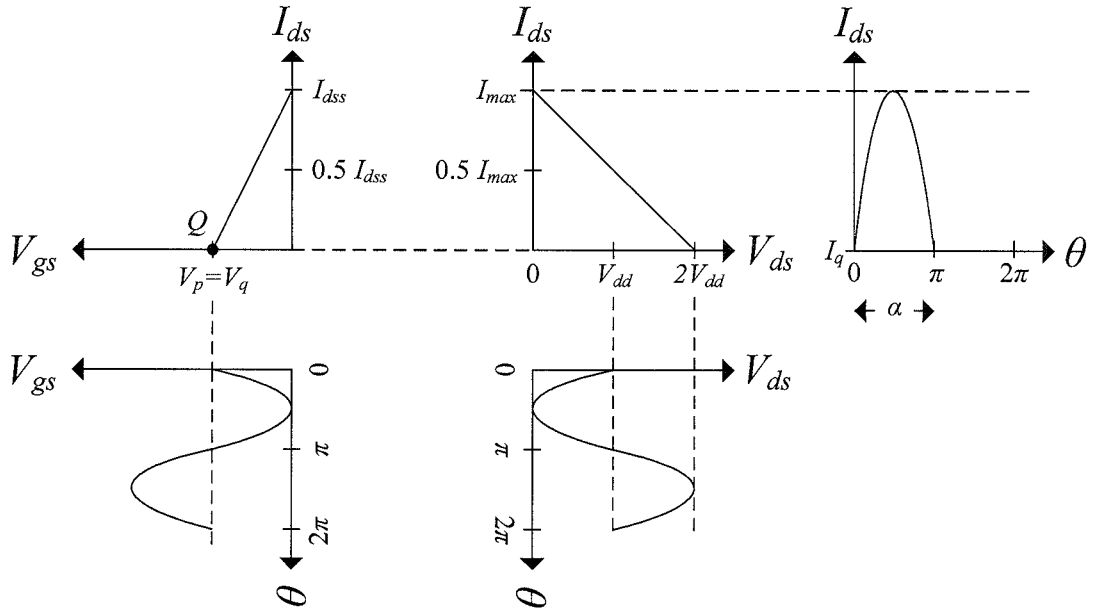


Figure 2.5: Voltage-current relationships for an ideal class-B PA.

For class-C PA (see Figure 2.6) the Q point is set below the pinch off voltage V_p of the active device so that the conduction angle is less than 180°.

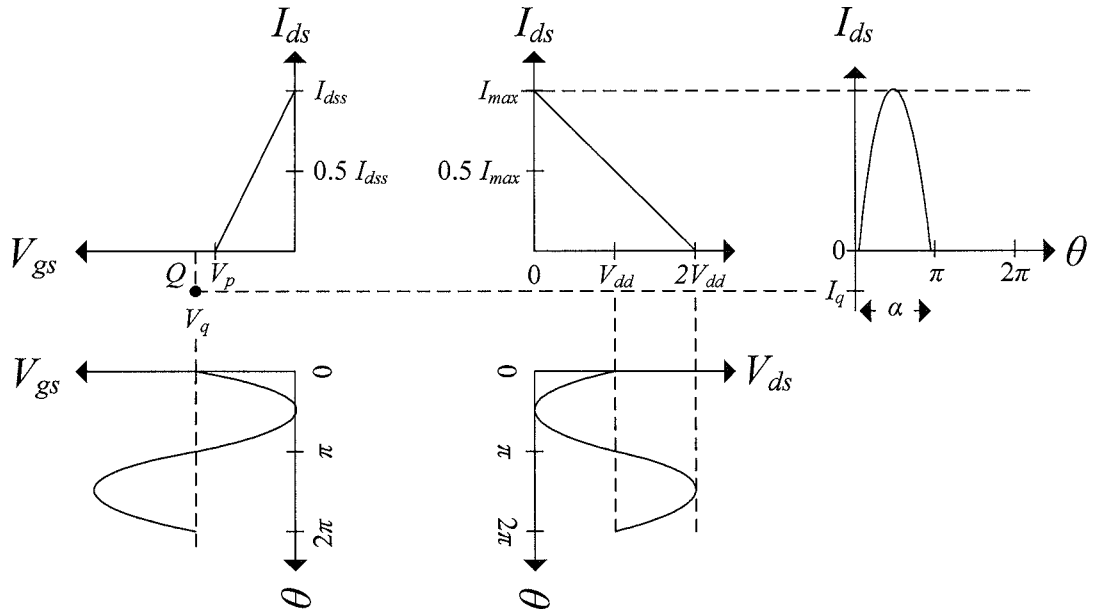


Figure 2.6: Voltage-current relationships for an ideal class-C PA.

The above conditions are summarised in Table 2.1.

Class	Quiescent voltage, V_q, V	Quiescent current, I_q, A	Conduction angle, α, degree
A	0.5 (V_{gs}=0-V_p)	0.5 I_{dss}	360
AB	$0 < V_q <$ (V_{gs}=0-V_p)	$0 < I_q <$ 0.5 I_{dss}	$180 < \alpha < 360$
B	V_p	I_{ds}=0	180
C	$<V_p$	I_{ds}<0	<180

Table 2.1: V_q, I_q and α of the class-A, AB, B, and C PAs.

In order to express the above voltage-current relationship analytically, a waveform analysis as a function of conduction angle is obtained [5]. Figure 2.7 shows the relationship between the gate voltage, V_{gs} and drain current, I_{ds}, where the ac input signal, $v_{gs}= V_s \cos \theta$.

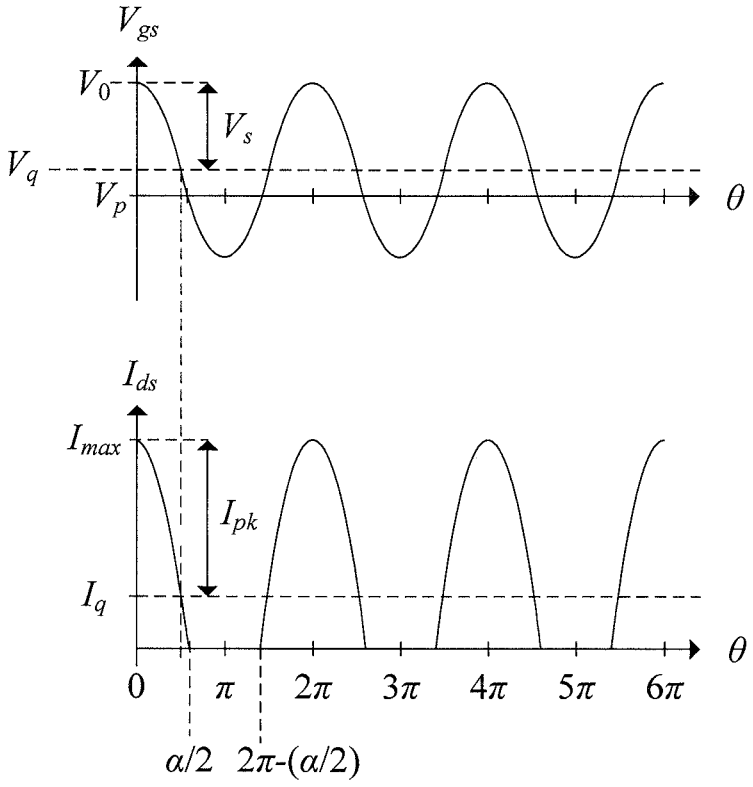


Figure 2.7: V_{gs} and I_{ds} waveforms of the class-A, AB, B, and C PAs.

From Figure 2.7, $V_{gs}(\theta) = V_q + V_s \cos\theta$. When $\theta = 0$ then $V_{gs} = V_0 = V_q + V_s$. To simplify the analysis, it is assumed that V_0=1, hence

$$V_s = 1 - V_q \tag{2.5}$$

where, V_s is the signal voltage. The lower the value of V_q, the larger the value of V_s becomes, and, the drain current becomes a truncated sinusoidal waveform, as shown in Figure 2.7.

When the transistor is conducting, the drain current is given by

$$i_{ds}(\theta) = I_q + I_{pk} \cos\theta \qquad 0 \le \theta < \alpha/2; \quad 2\pi - \alpha/2 < \theta \le 2\pi \tag{2.6a}$$

and, for the transistor in the 'off' condition, the drain current is

$$i_{ds}(\theta) = 0 \qquad \alpha/2 \le \theta \le 2\pi - \alpha/2 \tag{2.6b}$$

From equation (2.6a) when θ=0, $i_{ds}(\theta)$=I_{max}, then

$$I_{pk} = I_{\max} - I_q \tag{2.7}$$

where, I_{pk} is the amplitude of the sinusoidal input signal.

When $\theta = \alpha/2$, $i_{ds}(\theta)=0$, then

$$I_q = -I_{pk}\cos(\alpha/2) \tag{2.8}$$

hence, the conduction angle is given by

$$\alpha = 2\cos^{-1}\left(\frac{-I_q}{I_{pk}}\right). \tag{2.9}$$

Substituting equation (2.8) into the equation (2.7), I_{pk} and I_q can be written in terms of I_{max}, to give

$$I_{pk} = \frac{I_{\max}}{1-\cos(\alpha/2)} \tag{2.10}$$

and,

$$I_q = I_{\max}\cdot\frac{\cos(\alpha/2)}{\cos(\alpha/2)-1}. \tag{2.11}$$

Equation (2.6a) for drain current can then be written in term of I_{max}, as

$$i_{ds}(\theta) = I_{\max}\cdot\frac{\cos\theta-\cos(\alpha/2)}{1-\cos(\alpha/2)}. \tag{2.12}$$

The Fourier cosine series of drain current can then be written in term of I_{max} as

$$i_{ds}(\theta) = I_{dc} + I_1\cos\theta + I_2\cos 2\theta + I_3\cos 3\theta + \ldots \tag{2.13}$$

where, the first four coefficients are given by

$$I_{dc} = \frac{I_{\max}}{2\pi}\cdot\frac{2\sin(\alpha/2)-\alpha\cos(\alpha/2)}{1-\cos(\alpha/2)} \tag{2.14}$$

$$I_1 = \frac{I_{\max}}{2\pi}\cdot\frac{\alpha-\sin\alpha}{1-\cos(\alpha/2)} \tag{2.15}$$

$$I_2 = \frac{I_{\max}}{2\pi}\cdot\frac{\sin(\alpha/2)-\frac{1}{3}\sin(3\alpha/2)}{1-\cos(\alpha/2)} \tag{2.16}$$

$$I_3 = \frac{I_{\max}}{6\pi}\cdot\frac{(1-\cos\alpha)\sin\alpha}{1-\cos(\alpha/2)}. \tag{2.17}$$

Figure 2.8 shows the relative amplitudes of the first four drain current components for the class-A, AB, B, and C PAs as a function of the conduction angle (see Table 2.1). The I_{max} is assumed to be 1 A.

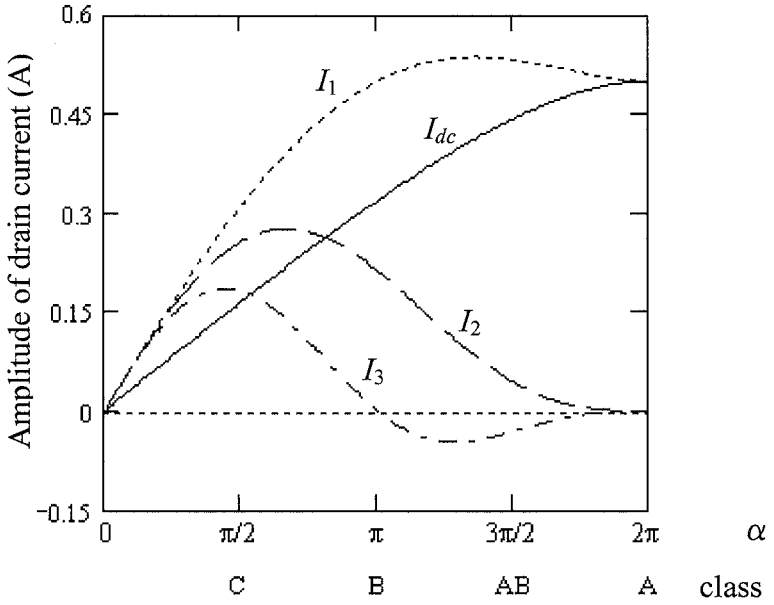


Figure 2.8: Amplitude of I_{dc}, I_1, I_2, and I_3 when I_{max}=1 A.

Over the class range C to A, the dc component, I_{dc} increases from zero to 0.5 A. The amplitude of the fundamental component, I_1, is a maximum in the class-AB range. For all classes, the fundamental, I_1, and the second harmonic, I_2, are in phase, while the third harmonic, I_3 is in phase with I_1 only for class-B and C, but is out of phase in the class-AB range. This latter property is beneficial in the implementation of class-F PAs as discussed in Section 2.6.

Using equation (2.14), the dc power supplied is given by

$$P_{dc} = I_{dc}V_{dd} = \frac{I_{\max}}{2\pi}\left(\frac{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}{1-\cos(\alpha/2)}\right)V_{dd}. \tag{2.18}$$

The current component of the fundamental frequency is given by equation (2.15) and hence the output power at the fundamental frequency is given by

$$P_{out} = \frac{V_{dd}I_1}{2} = \frac{I_{\max}}{4\pi}\left(\frac{\alpha - \sin\alpha}{1-\cos(\alpha/2)}\right)V_{dd}. \tag{2.19}$$

The drain efficiency is then given by

$$\eta_d = \frac{P_{out}}{P_{dc}} = \frac{1}{2}\left(\frac{\alpha - \sin\alpha}{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}\right). \tag{2.20}$$

Using equations (2.18), (2.19), (2.20), the graphs of P_{dc}, P_{out} and η_d, as a function of the conduction angle are shown in Figures 2.9 and 2.10.

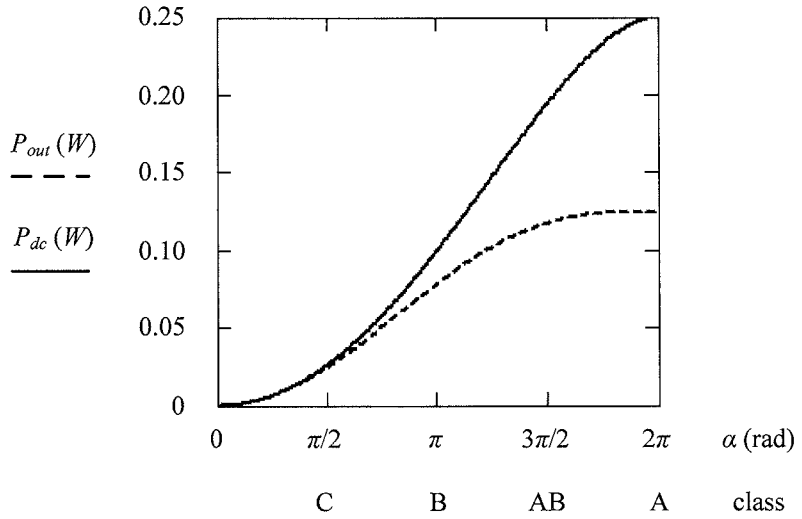


Figure 2.9: P_{dc} and P_{out} as a function of α for the class-A, AB, B, and C PAs.

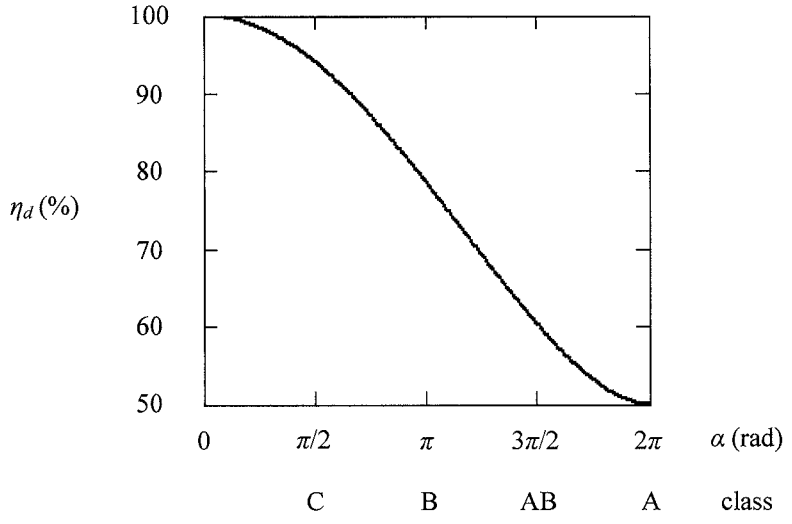


Figure 2.10: η_d as a function of α for the class-A, AB, B, and C PAs.

From the Figures 2.9 and 2.10, for the class-A PA, only one-half of the dc power is converted to ac output power and the other half is lost as heat, so the maximum theoretical drain efficiency is 50%. The value of the efficiency increases as the conduction angle is

reduced. For a class-B PA, a maximum drain efficiency of 78.5% can be obtained, while, for a class-C PA it is 100%. The output power for the class-C PA is very low. The class-AB PA has a better drain efficiency than the class-A PA, a higher gain, and is more linear than the class-B PA. However, in practice, the drain efficiency of class-A PA is reduced significantly to about 35% for L-band applications while L-band class-B can only achieve a drain efficiency to about 60% [15]. Although class-C PA can achieve higher efficiency it has a very low output power capability which results in not suitable for high frequency applications. The performances of these PAs is summarised in Table 2.2.

	Class-A	Class-AB	Class-B	Class-C
Drain efficiency, η_d	Low	Moderate	High	Very high
AC Output power, P_{out}	High	High/Moderate	Moderate	Low
Power Gain, G_p	High	High/Moderate	Moderate	Low
DC power, P_{dc}	Very high	High/Moderate	Low	Very low
Linearity	Very good	Moderate	Poor	Very poor

Table 2.2: Performances of class-A, AB, B, and C PAs.

From the above results it can be seen that as the transistor is biased toward the class-C, the conduction angle for drain current decreases, hence the mean, or, dc current decreases. This reduces the dc power supplied. In the extreme position of the bias point for a class-C PA, the theoretical drain efficiency can approach 100% but the output power approaches zero. The following section reviews the design of high efficiency PAs (class-D, E, and F) where the objectives of the design is to ensure that the drain current and voltage do not overlap, and so minimise the power dissipated in the transistor.

2.5 Review of High Efficiency PAs

For the class-AB and B PAs the drain current is a truncated sinusoidal waveform while the drain voltage is a sinusoidal waveform whose amplitude depends on the output load at the fundamental frequency. For maximum output power the load line is adjusted,

allowing the drain voltage to have a maximum voltage swing between the ohmic and saturation regions. However the power dissipated in the active device is considerable due to the overlapping area between the drain current and voltage waveforms. Consequently there is always a trade-off between the output power and the drain efficiency.

To improve the efficiency it is necessary to minimise the amount of power dissipated in the active device by ensuring that the overlapping area between the drain voltage and current waveforms is minimised. There are several types of high efficiency PAs [4], the most popular types being the class-D, E, and F, which are briefly reviewed in the following sub-sections. In Section 2.6 the theoretical analysis of an ideal class-F PA is discussed.

2.5.1 Class-D PA

In a class-D PA, two active devices, A and B (see Figure 2.11) behave as switches, which are alternatively switched 'on' and 'off' by the input drive signal.

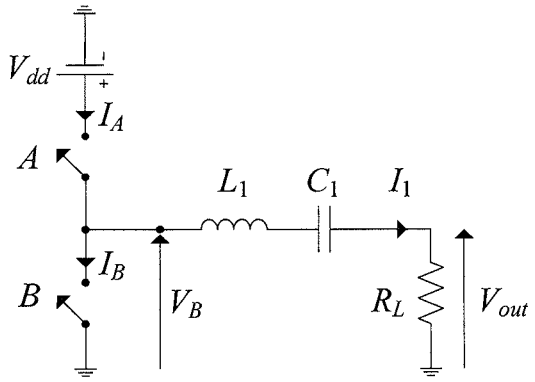


Figure 2.11: Circuit diagram of an ideal class-D PA.

A series tuned circuit (L_1C_1) is used at the output of the active devices to ensure that only the current at the fundamental frequency I_1 is present in the load resistance R_L. The resultant drain voltage V_B and current I_B are zero in each alternate half cycle as shown in

Figure 2.12, hence no power is dissipated in the active device, and a theoretical drain efficiency of 100% can be achieved.

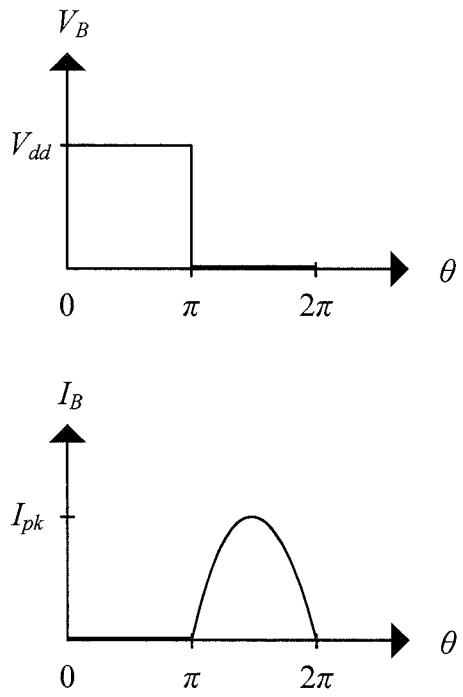


Figure 2.12: V_B and I_B waveforms of the class-D PA.

However, in practice, losses occur due to the saturation, switching speed and drain capacitance. These losses increase as the frequency increases, hence, class-D PAs are normally used in the LF, MF, HF ranges [16], [17] and only rarely in the VHF range [18] in high efficiency applications. To eliminate the losses due to the drain capacitance, a single active device with a shunt capacitance as a class-E PA was introduced by Sokals in 1975 [19], and, is discussed in the following sub-section.

2.5.2 Class-E PA

In a class-E PA a single active device (see Figure 2.13) is switched 'on' and 'off' by the input drive signal.

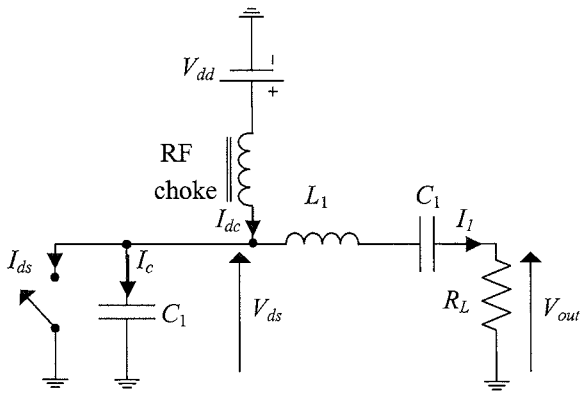


Figure 2.13: Circuit diagram of an ideal class-E PA.

A series tuned circuit (L_1C_1) is used to ensure that only the fundamental current flows in the load resistance R_L. The resulting drain current and voltage waveforms for an ideal class-E PA are shown in Figure 2.14.

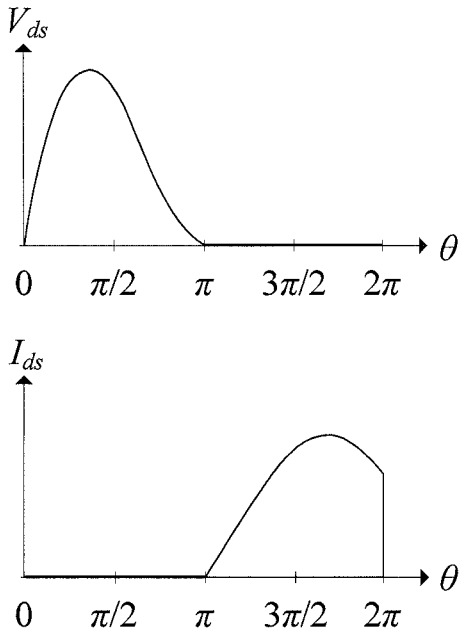


Figure 2.14: V_{ds} and I_{ds} waveforms of the class-E PA.

For the ideal class-E PA, when the active device is switched 'on' the drain voltage drops to zero and has a zero slope whilst the current flows through the switch. When the active device is switched 'off', no current flows through the switch but through the

capacitor, C_1. Consequently as the losses due to the charging of the drain capacitance are eliminated for an ideal PA, a theoretical drain efficiency of 100% can be obtained at higher frequencies [19], [20], which is not possible in the class-D PA. However, the maximum output power is limited to $0.577V_{dd}^2/R_L$ [1] for an ideal PA.

For the above high efficiency PAs (class-D and E), the active device is assumed to have an infinite "off" impedance and zero "on" impedance, and so a theoretical efficiency of 100% can be obtained. However, a practical active device has parasitic reactance, transition time, and turn-on resistance, which degrades the efficiency. Also in the RF and microwave frequency ranges the active devices are not able to switch fast enough due to the drain capacitance and lead inductance which degrade the efficiency. This restriction has been reported in [21] where three class-E PAs using the same MESFETs device were designed to operate at 0.5 GHz, 1 GHz and 2 GHz respectively. These PAs demonstrate a PAE of 80% at 0.5 GHz, a PAE of 73% at 1 GHz, and a PAE of 54% at 2 GHz. A class-F PA has the advantage since it uses multiple resonators at the output of the active device to obtain a high efficiency and a high output power at higher frequencies.

2.5.3 Class-F PA

An ideal class-F PA shown in Figure 2.15 can produce a theoretical drain efficiency of 100% with a higher output power.

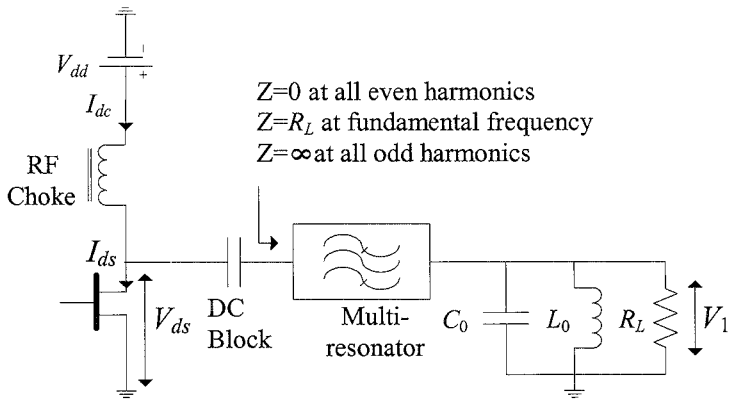


Figure 2.15: Circuit diagram of an ideal class-F PA.

This high efficiency is achieved by shaping the drain waveforms using a number of harmonic resonators. For the ideal PA with infinite resonators, zero load impedance at all the even harmonics and infinite load impedance at all the odd harmonics is obtained. Hence a square voltage waveform, and, a half-sinusoidal current waveform are produced (see Figure 2.16), which do not overlap. Hence no power is dissipated in the active device, and, also, there is an increase in the output power at the fundamental frequency. A theoretical drain efficiency of 100% is obtained.

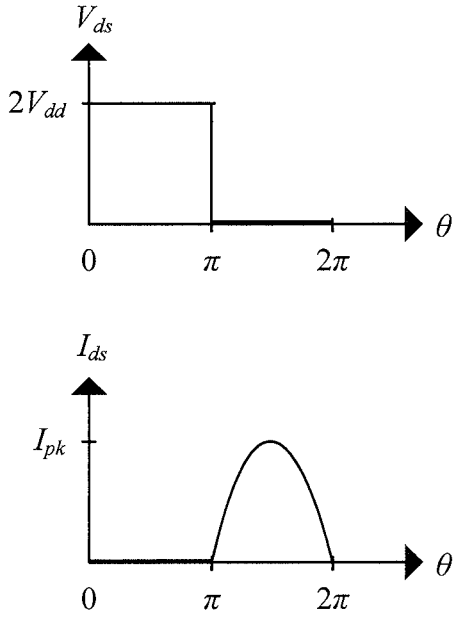


Figure 2.16: V_{ds} and I_{ds} waveforms of the class-F PA.

The early class-F PA designs using multiple resonators were introduced by Tyler [22] and extended by using lumped-element multi-resonator output networks for high-power A.M-broadcast transmitters, from LF through HF [23], [24]. At VHF and above, in order to overcome the difficulty of implementing these networks, Tyler proposed the use of quarter-wavelength transmission lines to control all the harmonics. In 1967, the first application of the class-F PAs operating at UHF was done by Snider [25], who proposed an optimally loaded PA in which all harmonic load impedances are either infinite or zero, with an overdriven active device.

In the following section an analysis of an ideal class-F PA with different combination of harmonics is discussed [26].

2.6 Theoretical Analysis of an Ideal Class-F PA

For a class-F PA using an infinite set of resonators, an ideal square voltage and a half-sinusoidal current waveforms are produced at the drain of the active device, as shown in Figure 2.16. The Fourier series of the drain voltage, V_{ds} and drain current, I_{ds}, are

$$V_{ds}(\theta) = V_{dd} + \frac{4}{\pi} \cdot V_{dd} \sum_{n=1,3,5...}^{\infty} \frac{\cos n\theta}{n} \tag{2.21}$$

$$I_{ds}(\theta) = I_{dc} - I_1 \sin\theta - I_2 \cos 2\theta - I_4 \cos 4\theta + ... \tag{2.22}$$

where, $I_1 = \frac{\pi}{2} I_{dc}$.

At the fundamental frequency, the output power is

$$P_{out} = \frac{V_1^2}{2R_L} = \left(\frac{4V_{dd}}{\pi}\right)^2 \frac{1}{2R_L} = \frac{8V_{dd}^2}{\pi^2 R_L} \tag{2.23}$$

and, the dc power supplied is

$$P_{dc} = V_{dd} \frac{8V_{dd}}{\pi^2 R_L} = \frac{8V_{dd}^2}{\pi^2 R_L} \tag{2.24}$$

where, $I_{dc} = \frac{8V_{dd}}{\pi^2 R_L}$.

The resulting drain efficiency is then given by

$$\eta_d = \frac{P_{out}}{P_{dc}} = \frac{8V_{dd}^2}{\pi^2 R_L} \cdot \frac{\pi^2 R_L}{8V_{dd}^2} = 100\%. \tag{2.25}$$

The ideal class-F PA having an infinite number of resonators is unrealistic in a practical design. In the practical case, only two or three resonators are used, and, the drain voltage is represented by either the first three or four Fourier terms. This results in either a third harmonic-peaking circuit (3rd HP), or, a fifth harmonic-peaking (5th HP) circuit, being employed in the design [26]. In the analysis, a maximally flat waveform is obtained by substituting the appropriate waveform coefficients into the voltage waveform, so the waveform becomes flattened at both the bottom and the peak. This produces a higher output voltage V_{out} component at the fundamental frequency, which results in a higher output power and drain efficiency.

In the analysis shown below, it is assumed that the drain current waveform is an ideal half-sinusoidal waveform. For 3rd HP circuit, the Fourier series for the drain voltage waveform, which takes into account only the fundamental and third harmonic components, can be expressed in the form

$$V_{ds}(\theta) = V_{dd} + V_1 \sin\theta + V_3 \sin 3\theta. \tag{2.26}$$

The half-sinusoidal drain current waveform is given by

$$I_{ds}(\theta) = I_{dc} - I_1 \sin\theta - I_2 \cos 2\theta - I_4 \cos 4\theta + \ldots \tag{2.27}$$

where, $I_1 = \frac{\pi}{2} I_{dc}$.

To obtain a maximally flat voltage waveform (see Figure 2.17), the ratio of the magnitudes of the fundamental voltage V_1, and, the third harmonic voltage V_3, in terms of

V_{dd}, are $V_1=(9/8)V_{dd}$ and $V_3=V_{dd}/8$ [26]. Substituting for V_1 and V_3 into equation (2.26), gives the drain voltage waveform for the 3rd HP shown in Figure 2.17.

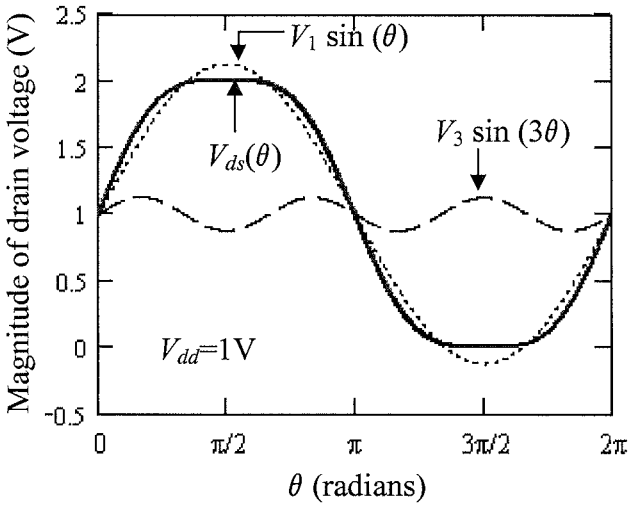


Figure 2.17: V_{ds} waveform for the 3rd HP circuit.

At the fundamental frequency, the output power is

$$P_{out} = \left(\frac{9V_{dd}}{8}\right)^2 \frac{1}{2R_L} = \frac{81V_{dd}^{\ 2}}{128R_L} \tag{2.28}$$

and, the dc power supplied is

$$P_{dc} = V_{dd} I_{dc} = \frac{9V_{dd}^{\ 2}}{4\pi R_L} \tag{2.29}$$

where, $I_{dc} = \dfrac{9V_{dd}}{4\pi R_L}$.

The resulting drain efficiency is

$$\eta_d = \frac{P_{out}}{P_{dc}} = 88.4\%. \tag{2.30}$$

For 5th HP circuit, a further resonator is used to tune the fifth harmonic load impedance. The voltage across the active device is then

$$V_{ds}(\theta) = V_{dd} + V_1 \sin\theta + V_3 \sin 3\theta + V_5 \sin 5\theta. \tag{2.31}$$

The half-sinusoidal drain current waveform is

$$I_{ds}(\theta) = I_{dc} - I_1 \sin\theta - I_2 \cos 2\theta - I_4 \cos 4\theta + \ldots \tag{2.32}$$

where, $I_1 = \frac{\pi}{2} I_{dc}$.

For a maximally flat waveform, the ratio of the magnitudes of fundamental, third and fifth harmonic voltages with respect to the dc voltage, V_{dd} are V_1=(75/64)V_{dd}, V_3=(25/128)V_{dd} and V_5=(3/128)V_{dd} [26]. Substituting these values V_1, V_3, and V_5 into equation (2.31), gives the drain voltage waveform for the 5th HP circuit as shown in Figure 2.18.

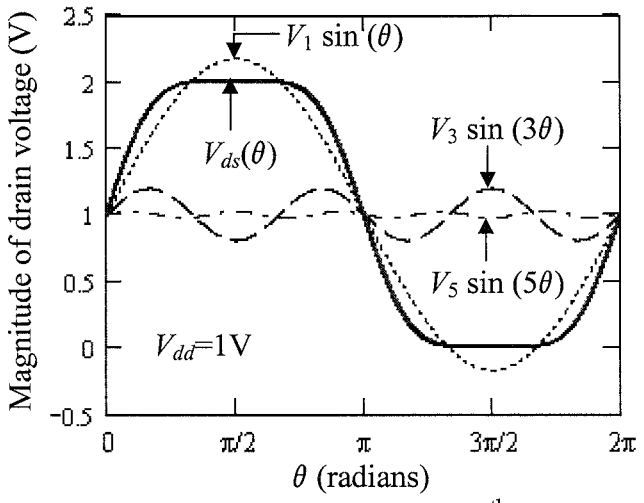


Figure 2.18: V_{ds} waveform for the 5th HP circuit.

At the fundamental frequency, the output power is

$$P_{out} = \frac{5625 V_{dd}^{\ 2}}{8192 R_L} \tag{2.33}$$

and, the dc power supplied is

$$P_{dc} = V_{dd} I_{dc} = \frac{75 V_{dd}^{\ 2}}{32\pi R_L} \tag{2.34}$$

where, $I_{dc} = \frac{75 V_{dd}}{32\pi R_L}$.

The resulting drain efficiency is then

$$\eta_d = \frac{P_{out}}{P_{dc}} = \frac{5625V_{dd}^{\ 2}}{8192R_L} \cdot \frac{32\pi R_L}{75V_{dd}^{\ 2}} = 92\%. \tag{2.35}$$

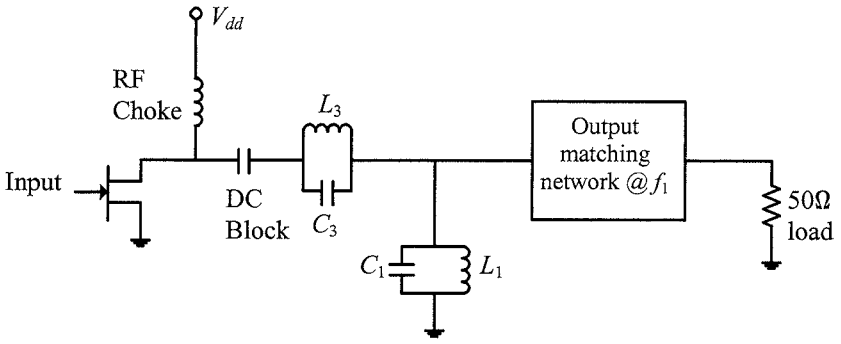
A summary of the performances of the class-A, B, and F PAs, is given in Table 2.3.

	A	B	3rd HP	5th HP	Ideal class-F
Number of harmonic at V_{ds} waveform	1	1	3	5	∞
Number of harmonic at I_{ds} waveform	1	∞	∞	∞	∞
Maximum ideal drain efficiency, η_d (%)	50	78.5	88.4	92	100

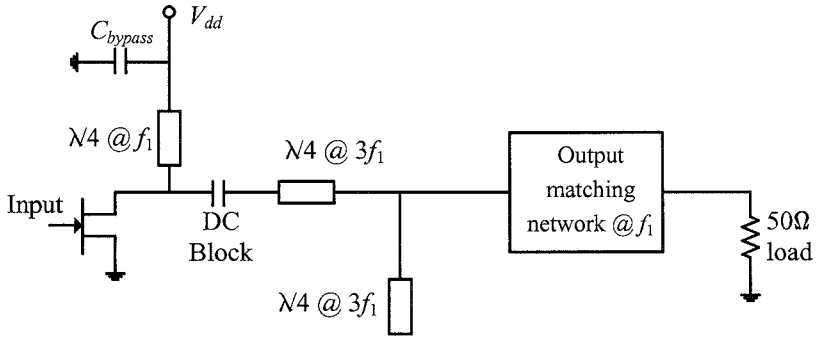
Table 2.3: Performances of class-A, B, and F PAs with various combinations of harmonics.

The drain efficiency of an ideal class-F PA increases from the 50% limit of class-A PA to 100%, depending on the number of harmonics controlled. In the case of the 3rd HP circuit, the drain efficiency is approximately 10% higher than in the class-B PA, which is a significant improvement in terms of output power, and, also relaxes the cooling requirement. On the other hand, a 5th HP circuit is approximately 4% higher than a 3rd HP circuit, but has a more complicated circuit. Consequently there is a trade-off between the complexity of the circuit and efficiency, so the 3rd HP circuit is normally preferred.

Figure 2.19 shows two examples of the topologies that can be used in the 3rd HP output circuit [27]. The lumped element topology is shown in Figure 2.19(a) and the transmission line topology is shown in Figure 2.19(b).



(a)



(b)

Figure 2.19: 3rd HP circuits. (a) Lumped element. (b) Distributed element.

In Figure 2.19(a), the parallel tuned circuit (L_3C_3), which is located in series with the drain terminal, has a high impedance at the third harmonic, and, a low impedance at all other harmonics. The parallel tuned circuit (L_1C_1), ensures that only the fundamental current flows in the 50 Ω load. To obtain a maximum output power, an output matching network is used to match the required optimum load impedance to the 50 Ω load. In the transmission line 3rd HP circuit a λ/4@f_1 line is used to produce short circuit terminations at all the even harmonics. Two λ/4@3f_1 lines are used to produce an open circuit load termination at the third harmonic. In the same way, for maximum output power an output matching network is added to match the optimum load impedance to the 50 Ω load.

Class-E and F PAs have their advantages and disadvantages. The class-E PAs have a simpler circuit compared to the class-F PAs. As shown in Figures 2.13 and 2.15, class-E PAs only use an output capacitance, C_1 and a simple output matching network for their switching operation, whereas class-F PAs need a number of resonators to control the odd harmonics, which increases the circuit complexity. Additionally, class-E PAs have the advantage of incorporating the intrinsic capacitance of the transistor, e.g., C_{ds} into the circuit topology. For class-F PAs, there could be a problem if there is a large drain intrinsic capacitance as this would stop the higher harmonics having an open-circuit at the drain. The class-E PAs also utilise the output capacitance to eliminate discharge losses from this capacitor. Class-F PA also has the following advantages. First, more desirable waveforms

can be obtained with low peak voltage and mean current. Also higher output power can be obtained as compared with class-E PAs [28]. Additionally, the allowable maximum frequency in the class-E PAs is limited [21], because, above this maximum frequency, the class-E PAs will operate in sub-optimum mode. For the class-F PAs, the intrinsic capacitance is not the crucial parameter for determining the allowable maximum frequency, and so the class-F PAs are capable of operating at higher frequencies.

2.7 Summary

The development of the solid-state power devices has been discussed and their performance has been closely linked to the newly developed semiconductor material and advances in processing technology. These solid-state devices have had a major impact upon the development of microwave and millimetre-wave systems.

The design parameters of a PA and the waveform analysis for ideal class-A, AB, B, and C PAs have been presented. To improve the drain efficiency of the linear class-A PA, the active device is biased beyond the one-half of the current I_{dss}, which results in an increase in efficiency from 50% to 78.5% for an ideal class-B PA, and, to 100% for an ideal class-C PA. However, the high efficiency of class-C PA comes at the price of very low output power. Moreover, in practice for L-band application class-A PA can achieve an efficiency of about 35% while class-B PA can achieve an efficiency of about 60%. Also at these high frequencies, the very low output power class-C PA is not desirable. Hence, the high efficiency PAs (class-D, E, and F) are more attractive to PA designers since they can obtain higher efficiency in both the theoretical (100%) and practical (>60%) cases.

For the ideal class-D and E PAs, the transistor acts as a switch, and, with the designed load networks, the power dissipated in the active device is zero, and hence, a theoretical drain efficiency of 100% is obtained. However in the RF and microwave frequency ranges the active devices are restricted by the switching speed due to the drain

capacitance and lead inductance, which degrade the efficiency. This is not the case for class-F PA and hence this is preferred in this thesis. Class-F PAs offer a high efficiency performance by having the possibility of controlling the impedances at a finite number of harmonics [26]. For the ideal class-F PA, multiple resonators are utilised to obtain non-overlap drain current/voltage waveforms. The resultant waveforms show simultaneous minimisation of the power dissipated in the active device, and, a maximisation of the output power at the fundamental frequency. The circuit topologies and theoretical analysis for an ideal class-F PAs have been discussed. However in the practical case the parasitic reactance of the device packages, the nonlinearities of the drain current, and, the gate, and, also the drain capacitances, must be taken into account. Hence it is necessary to employ the load/source-pull method to determine the optimum load and source impedances which is discussed in Chapter 3. Practical circuit topologies are required to realise the optimum impedances in order to obtain a high efficiency performance. This is discussed in Chapters 4 and 5.

CHAPTER 3 NONLINEAR MODELLING OF FETS AND DETERMINATION OF HARMONIC SOURCE AND LOAD IMPEDANCES FOR MAXIMUM EFFICIENCY

3.1 Introduction

As discussed in Chapter 2 in order to improve the efficiency of the dc to ac power conversion in PAs a large input signal is normally applied to an active device to switch it 'on' and 'off'. Consequently, it is necessary to use a nonlinear model of the active device and a corresponding nonlinear analysis in order to determine the optimum source and load harmonic impedances for maximum PAE [29].

In Section 3.2 a brief review is presented of the dc and ac nonlinear models which includes the Statz model of a FET [6], [30], [31]. Also the different analytical techniques employed including the power series, Volterra series, and, harmonic balance (HB) methods [32] are discussed.

For the FET (ATF34143) used in this thesis, the parameters of the Statz model are evaluated. This model is then used in Section 3.3 to investigate the stability of this active device which limits the range of load/source impedances that can be used in the design of the PA. In this section the conditions and formulas are given for determining the frequency range over which the active device is unconditionally stable in terms of S-parameters [33], [34]. These formulas are then applied to determine the frequency range over which the FET (ATF34143) is unconditionally stable. It is shown that this particular active device is not stable over the required range of the PA harmonic frequencies. The effect on stability by placing a resistor at the gate terminal of the FET is investigated.

A practical FET is a non-unilateral device so that the load and source impedances are interdependent. Hence a load/source-pull method [35] is normally used to obtain the

optimum source and load impedances required to produce maximum PAE. This method is discussed in detail in Section 3.4.

In Section 3.5 a novel application of the load/source-pull method is applied to determine the optimum load and source impedances for class-F PAs (using the ATF34143) at the fundamental, second, and third harmonics. These impedances transform the input sinusoidal voltage signal into optimum waveforms at the gate and drain terminals of the FET, so that, a maximum PAE can be obtained. Based on this work three papers have been published in [36]-[38].

3.2 Review of AC and DC Nonlinear Modelling

3.2.1 AC nonlinear models of FETs

A simplified nonlinear equivalent circuit of an FET is shown in Figure 3.1 where it is assumed that the device operates as a voltage controlled current source in the active mode.

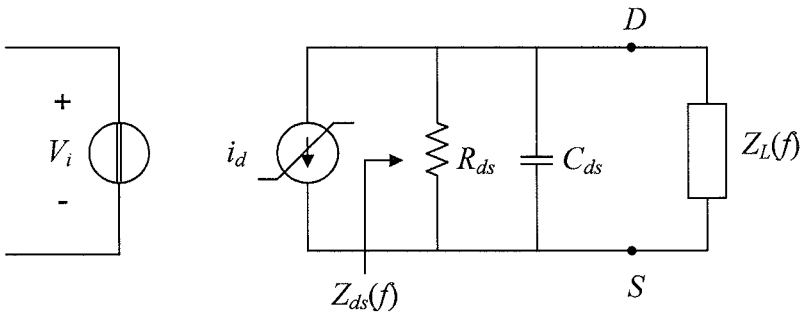


Figure 3.1: Simplified nonlinear equivalent circuit of an FET.

In this model, the only nonlinear characteristic of the active device is the voltage controlled current source. The effects of the reciprocity property, pinch-off, and drain current saturation, have been neglected. Hence the model is only valid over a limited frequency range, but, provides an initial indication of the performance of the PA [31].

For maximum efficiency the drain voltage, is optimally shaped by using harmonic load impedances, while the source impedance is the complex conjugate of the large signal

input impedance at the fundamental frequency. These impedances are obtained by expressing the drain current, I_{ds}, and, the drain voltage, V_{ds} in terms of Fourier series as given by [39]

$$I_{ds}(\theta) = I_0 + \sum_{n=1}^{\infty} I_n \cos(n\theta + \xi_n) \tag{3.1}$$

$$V_{ds}(\theta) = V_{dd} - \sum_{n=1}^{\infty} V_n \cos(n\theta + \psi_n) \tag{3.2}$$

where,

$$V_n = Z_{ds,nf}\ e^{-j\varphi_n}\ I_n \tag{3.3}$$

and, ξ_n is the phase of the n^{th} harmonic component of the current, I_n, ψ_n is the phase of the n^{th} harmonic component of the voltage, V_n, ϕ_n=(ξ_n-ψ_n), $Z_{ds,nf}$ is the impedance across the drain to source device terminals. I_0 is the dc current component, and, V_{dd} is the dc voltage supplied. An expression for I_n as a function of the conduction angle is given in [40].

In the application of a CAD software tool a more accurate and efficient large-signal equivalent circuit is required, such as the model shown in Figure 3.2.

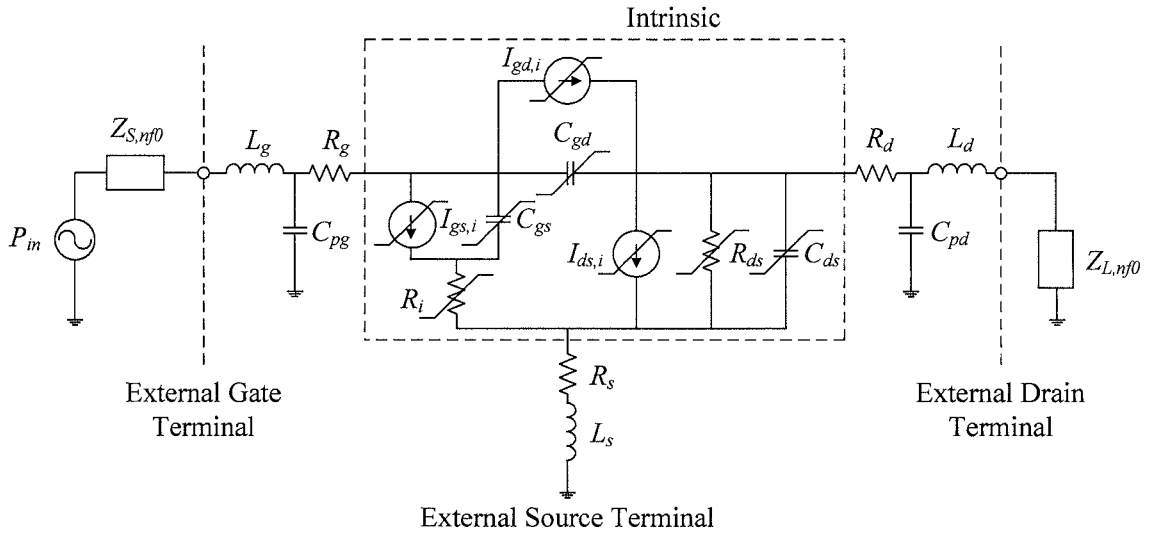


Figure 3.2: Large-signal equivalent circuit of an FET.

All the intrinsic circuit elements, R_{ds}, C_{ds}, C_{gs}, C_{gd}, R_i, $I_{gs,i}$, $I_{gd,i}$, and $I_{ds,i}$ are treated as nonlinear components while the parasitic elements, R_d, L_d, C_{pd}, R_g, L_g, C_{pg}, R_s, and L_s are assumed linear. As this model includes the non-unilateral property of the FET, the harmonic source and load impedances are interdependent and vary with the input power. The detailed process to determine these impedances for maximum PAE, using a novel application of the load/source-pull method, is discussed in detail in Section 3.5.

3.2.2 DC nonlinear models of FETs

A class-F PA is normally biased deep in the class-AB condition and hence it is important to have an accurate model of the pinch-off region of the device to obtain a more realistic simulation of the output power as a function of the input drive signal.

Curtice proposed a quadratic model [41] in which a square-law dependence of drain current on gate voltage is assumed. This model is simple but gives a poor fit to the transconductance, g_m characteristics so that it is in the only possible to include the first two harmonics in the output. Materka [42] then modified the Curtice model by including the effect of the drain voltage on the pinch-off voltage, in order to produce a soft pinch-off response. To improve the fitting of the transconductance characteristics of the Curtice quadratic model, a modified model was introduced by Curtice and Ettenberg [43]. In this model a third-order polynomial was proposed for the drain current as a function of gate voltage so that terms up to the third-order harmonic were included and the intermodulation distortion could more accurately be simulated.

In the Statz model for the FET [6], the capacitance formulas for C_{gs} and C_{gd} as functions of both the drain voltage and gate voltage were derived. Consequently, this model produces a very good fitting of the transconductance characteristics, and, hence, this model is normally used in the design of the mixers, Class-AB and Class-B PAs [30].

The manufacturing parameters of the FET (ATF34143) were inserted into the Statz model which was then simulated using the ADS software tool in order to obtain its dc characteristics. The simulated dc characteristics for the FET are shown in Figures 3.3 and 3.4.

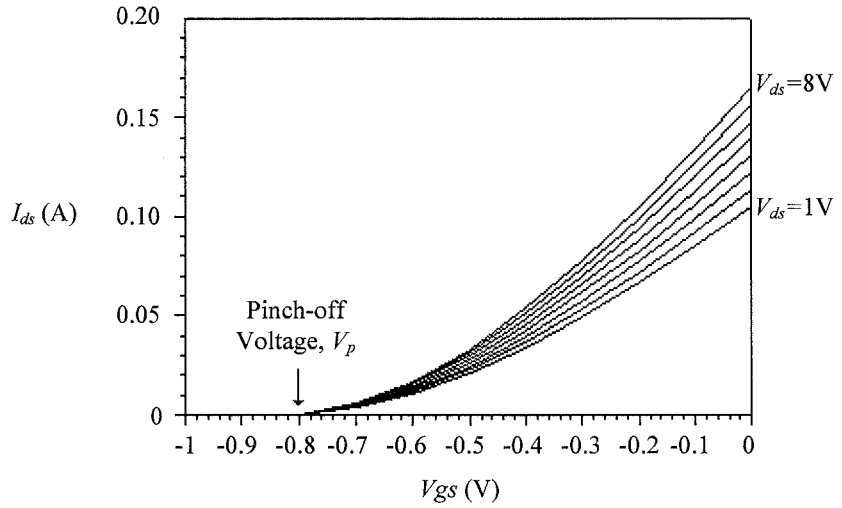


Figure 3.3: Simulated I_{ds}-V_{gs} characteristics of FET (ATF34143).

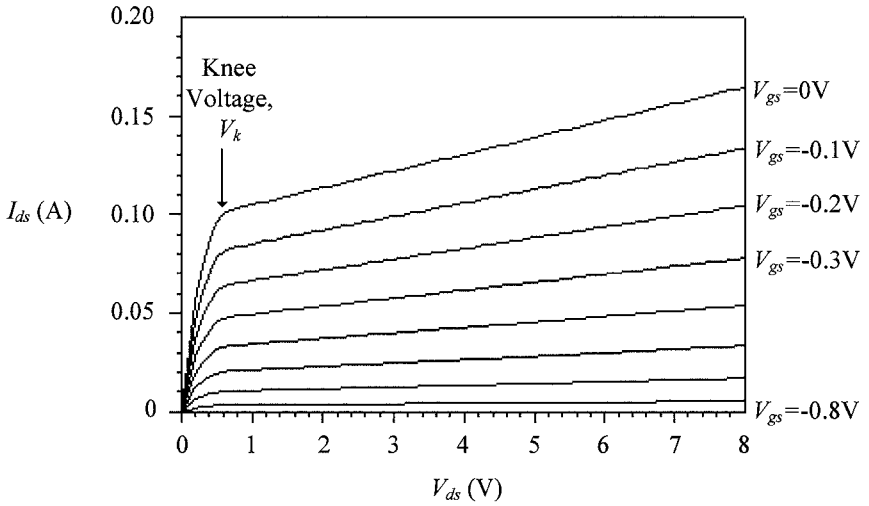


Figure 3.4: Simulated dc *I-V* curves generated with the Statz model.

In Figure 3.3 the drain voltage is increased in steps of 1 V from V_{ds}=1 V to V_{ds}=8 V while in Figure 3.4 the gate voltage is shown in steps of 0.1 V starting at the pinch-off voltage (V_p=V_{gs}=-0.8 V) to V_{gs}=0 V. The knee voltage, V_k for this device is approximately

0.6 V. The above dc *I-V* curves were then used to determine a suitable *Q* point. This model is used in Section 3.3 to examine stability, and, in Section 3.5 to obtain the optimum load and source impedances.

3.2.3 Nonlinear analytical methods

The power series, Volterra series, and harmonic balance (HB) are three popular methods used to analyse the nonlinear circuits [32]. The former two methods are normally used to analyse weak nonlinear circuits where the nonlinearity functions are limited to third order terms. The HB method can be used to analyse strong and weak nonlinear circuits excited by a single large-signal. The above three methods are briefly discussed below.

The power series method can only be applied to circuits which do not have a time delay caused by inductive or capacitive elements. The analysis is carried out in the frequency domain as this saves conversion time between the time and frequency domains. The nonlinearity of an element is expressed in polynomial form as a function of the input excitation signal [32], but only the amplitudes of the first three harmonics are obtained. This method is useful, as it provides an intuitive understanding of the behaviour of the nonlinear circuits in the generation of harmonics which cause intermodulation distortion. However, it has limited applications as saturation and threshold effects cannot be included.

Weak nonlinear circuits, which include the memory effects (time delay) can be analysed using the Volterra series to obtain the output responses as a function of both the amplitude and the phase of the input signal. However, the main disadvantage of this method is that the output is restricted to a maximum of third order terms because of the complexity of determining the nonlinear transfer functions (kernels) of higher order [44].

Strong nonlinear circuits with a single excitation, where higher order functions are present, are usually analysed using the HB method. In this thesis, a commercial software

tool ADS which includes the HB method is used to simulate the performance of all linear and nonlinear circuits. In general, the HB method can accurately produce steady state solutions of nonlinear circuits and systems fed by large periodic input signals. It is widely used in the design not only of PAs, but, also frequency multipliers, mixers, oscillators, and, modulators [45]. The method is briefly described below.

In the HB method the circuit is separated into linear and nonlinear sub-networks as shown in Figure 3.5. The analysis of the linear elements is carried out in the frequency domain while the nonlinear elements are analysed in time domain [32], [45].

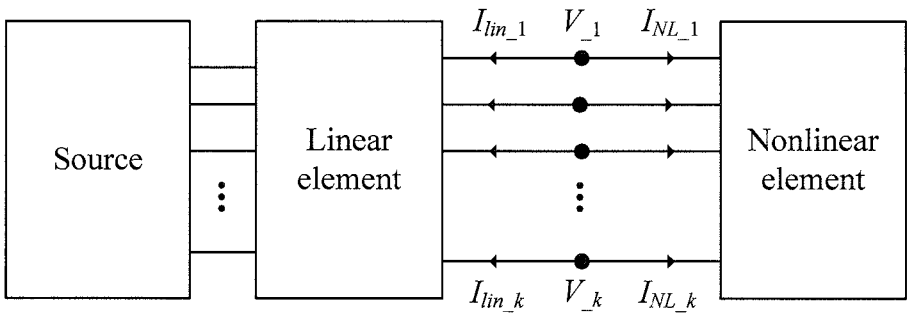


Figure 3.5: Partition representation of circuit for HB method.

In the analysis, the frequency domain excitation signal is transformed using the inverse Fourier transform and the currents flowing from nodes into nonlinear elements are determined. The currents flowing in the nonlinear circuits are then transformed to the frequency domain using the Fourier transform. The currents appearing in both the linear and nonlinear networks equations must sum to zero at the nodes for each harmonic. For the nonlinear components it is not possible to obtain a direct solution. Hence, an error function is employed to compute the sum of currents at all the nodes, and an iterative technique, such as Newton's method, is used to minimise the error. The voltage amplitudes and phases are then adjusted to minimise this error function. From an initial condition the iteration process is repeated until a solution is obtained within an acceptable minimum

error. This method is used in Section 3.5 with the load/source-pull method to determine the optimum harmonic source and load impedances, and, in Chapters 4 and 5 the method is used in the design of class-F PAs.

However, although maximum efficiency can be theoretically obtained it is also necessary to ensure that these impedances do not make the PA unstable. The criteria for stability are considered in the following section.

3.3 Stability Analysis

Low and RF frequency oscillations [46] can occur in PAs. The low frequency oscillations occur in the VHF frequency range and are mainly caused by the RF blocking capacitors used in the bias circuits. The RF oscillations are due to positive feedback caused by the non-unilateral properties of the active device.

Two parameters, the Rollett K-factor [33], and, the μ-factor [34] are normally used to determine if the active device is unconditionally stable. For unconditional stability the Rollett stability K requires two conditions [34]:

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}-S_{21}|} > 1 \tag{3.4}$$

where, $\Delta = S_{11}S_{22} - S_{12}S_{21}$. This condition, together with any one of the following five auxiliary conditions will ensure unconditionally stability.

$$1+|S_{11}|^2-|S_{22}|^2-|\Delta|^2 > 0 \tag{3.5a}$$

$$1-|S_{11}|^2+|S_{22}|^2-|\Delta|^2 > 0 \tag{3.5b}$$

$$|S_{11}S_{22}-S_{12}S_{21}| < 1 \tag{3.5c}$$

$$1-|S_{11}|^2 > |S_{12}-S_{21}| \tag{3.5d}$$

$$1-|S_{22}|^2 > |S_{12}-S_{21}| \tag{3.5e}$$

The μ-factor for unconditional stability at the load is

$$\mu_L = \frac{1-|S_{11}|^2}{|S_{22}-\overline{S_{11}}\Delta|+|S_{12}S_{21}|} > 1 \tag{3.6}$$

and, at the source is [34]

$$\mu_S = \frac{1-|S_{22}|^2}{|S_{11}-\overline{S_{22}}\Delta|+|S_{21}S_{12}|} > 1. \tag{3.7}$$

Since, condition (3.6) implies condition (3.7), and, vice versa, only one condition is needed [47].

The large signal S-parameters (LSSP) for the FET (ATF34143), were used to investigate the μ-factor stability over the frequency range 0.2-10 GHz as described below. The circuit used in the stability simulation is shown in Figure 3.6 and the load and source stability μ-factors, μ_L, μ_S, are plotted as a function of frequency as shown in Figure 3.7.

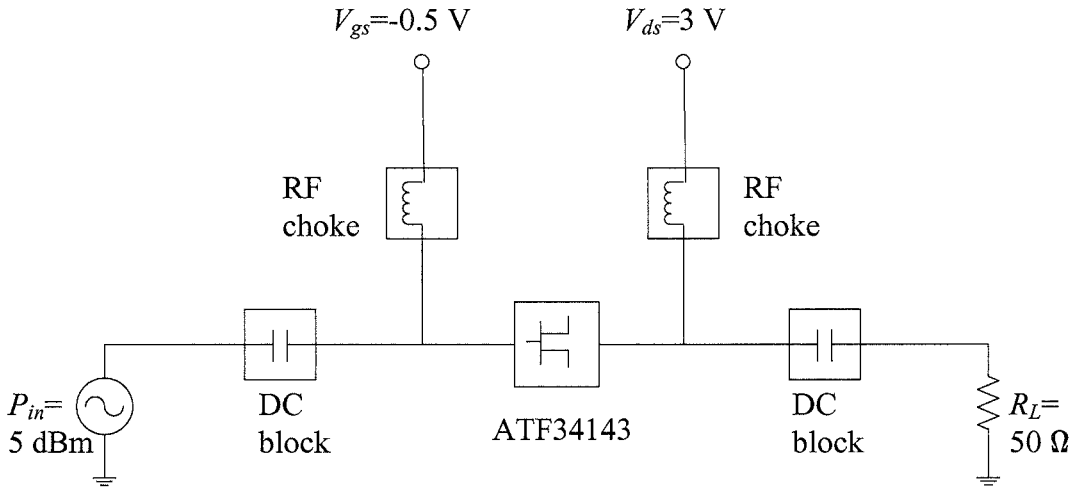
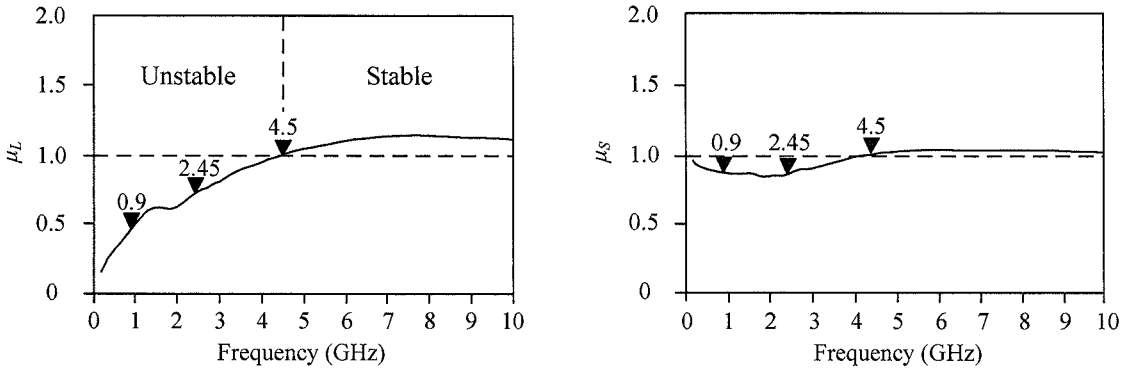


Figure 3.6: Stability simulation setup.



(a) (b)

Figure 3.7: μ-factors obtained from LSSP simulation. (a) Load. (b) Source.

As can be seen the source and load stability μ-factors are less than unity up to about 4.5 GHz and hence in this range the active device is unstable. Therefore a stabilising circuit is required to ensure that the FET is unconditionally stable over the required frequency range. The stability frequency range is improved by using a resistor connected directly to the gate terminal of the FET as shown in Figure 3.8. Stabilising resistors are not used in the output network as large signals cause the efficiency to drop rapidly.

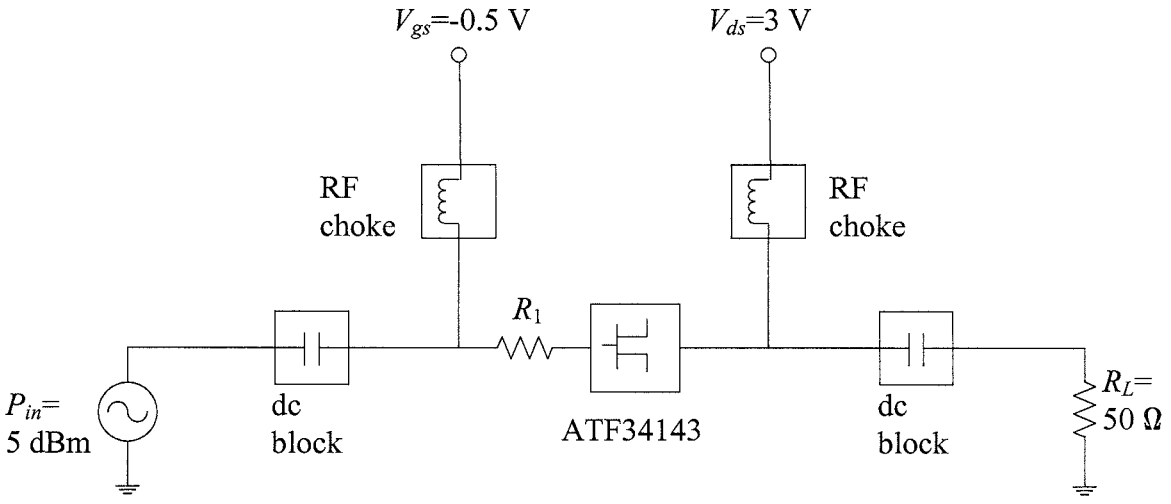
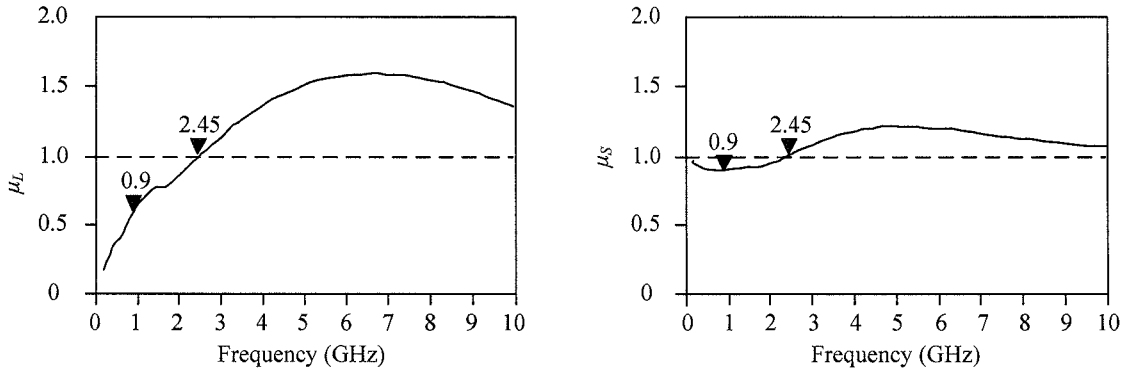


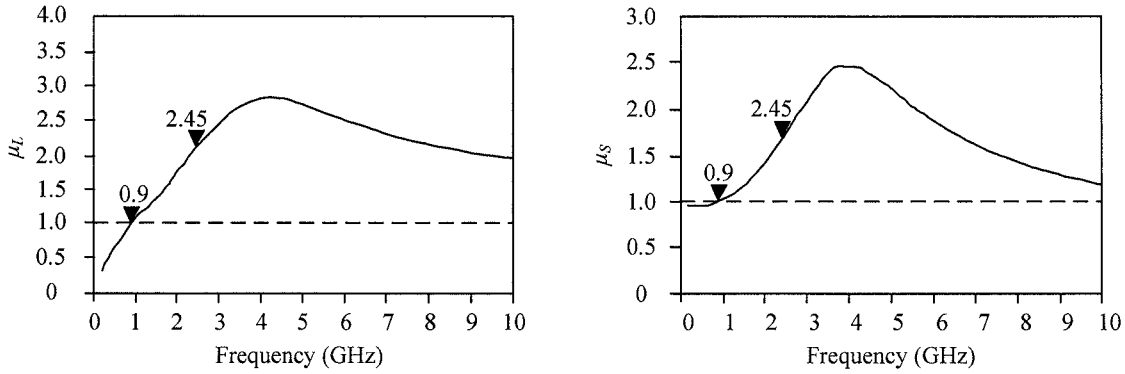
Figure 3.8: Stability simulation setup with a stabilising resistor.

Figures 3.9, 3.10, and 3.11 show the stability μ-factors at the input and output sides of the active device for the resistors, R_1=4.7 Ω, 22 Ω, and 150 Ω.



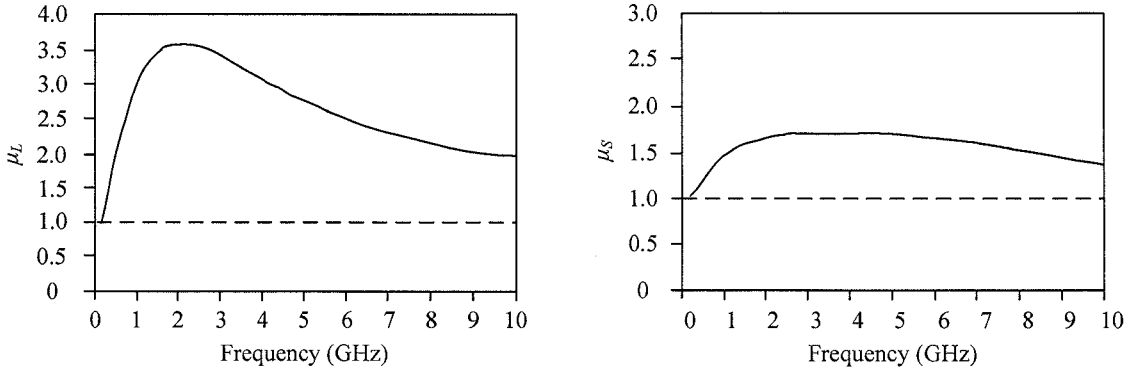
(a) (b)

Figure 3.9: μ-factors when R_1=4.7 Ω. (a) Load. (b) Source.



(a) (b)

Figure 3.10: μ-factors when R_1=22 Ω. (a) Load. (b) Source.



(a) (b)

Figure 3.11: μ-factors when R_1=150 Ω. (a) Load. (b) Source.

As can be seen from the above figures a resistor of 4.7 Ω is required to stabilise the frequency range from 2.45-10 GHz while the value of the resistor must be increased to 22 Ω to ensure the device is stable over 0.9-10 GHz, and, over the range 0.2-10 GHz a 150 Ω is required. These simulation results show that as the value of the resistor increases

the frequency range over which the device is stable also increases. However, as the value of the resistor increases the efficiency of the PA decreases and hence there is a compromise between the stability frequency range and efficiency. From the above graphs, as expected, it is seen that either of the source or the load μ-factors, μ_L, μ_S can be used in the stability analysis [47].

Using the appropriate stabilising resistor to ensure that the active device is stable in the required frequency range the optimum load and source impedances can be determined. These impedances are normally obtained using the load/source-pull method as discussed in the following section.

3.4 Load-Pull Method

The load-pull method shown in Figure 3.12 was first introduced in 1974 [48] as a practical method of measuring the optimum load impedance at a frequency, f_0, and, input power, P_{in}.

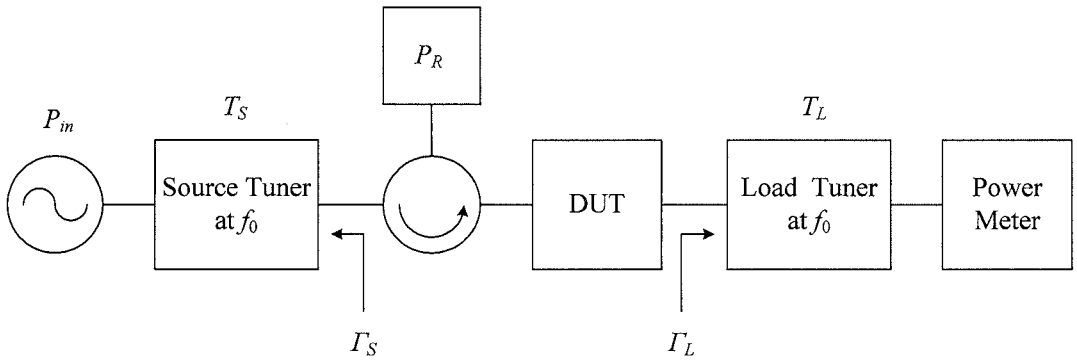


Figure 3.12: Basic block diagram for passive load-pull setup.

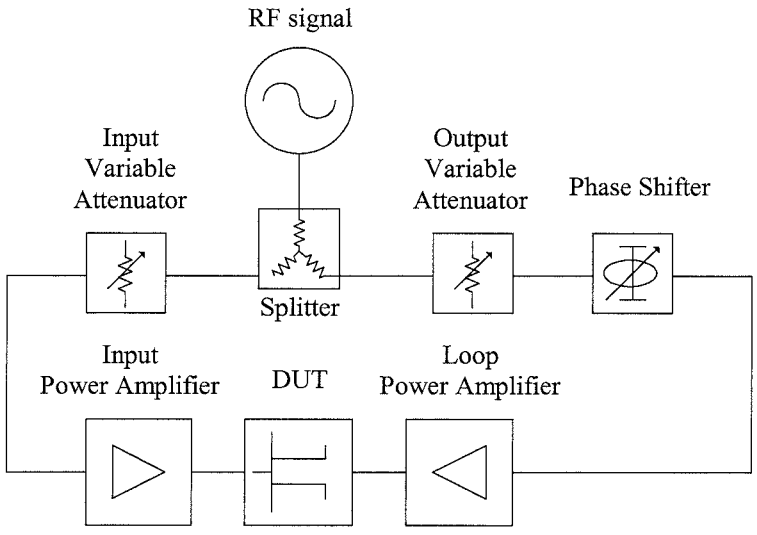
The tuners, T_L and T_S are adjusted so that the reflected power, P_R is minimal and the output power is optimum. For this condition the load and source impedances are then determined.

For manual measurements dielectric slug tuned air lines [48], slide-screw tuners [49], and, solid-state tuners [50] have been used. In computer controlled measuring systems

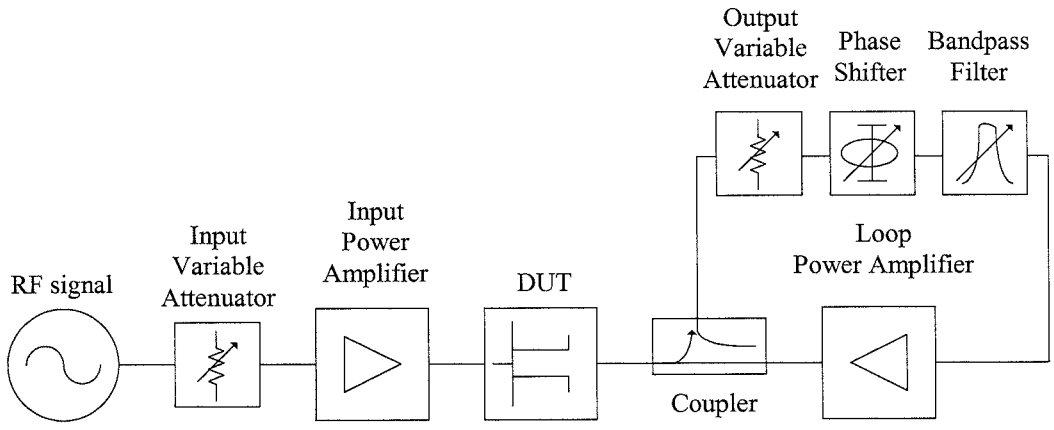
power meters are replaced by a vector network analyser to obtain measurements in real-time with much better accuracy [51].

At a fixed frequency and a varying input power the output tuner is adjusted and the above process repeated to obtain the resulting loci of impedances which are then displayed on Smith chart contours. From the contours the optimum impedance is obtained.

The importance of the harmonic load impedances in optimising the efficiency was reported in [25] and the above load-pull method was extended to the second harmonic [52], and, later, up to the fourth harmonic [53]. The harmonic load-pull method may use commercially available tuners such as triplexer [54], harmonic rejection tuners [55], or, multi-purpose tuners [56]. The method is easy to use, has a high power capability and is comparatively inexpensive. However, at higher frequencies the losses of the source and the load tuners increase and hence the accuracy of the measurement reduces. To overcome the problem, an active load system was introduced where the requirement for a physical impedance tuner was eliminated. Figures 3.13(a) and (b) show two typical test setups for active load systems based on the two-signal technique [57], and the active loop technique [58].



(a)



(b)

Figure 3.13: Block diagram for active load-pull setup. (a) Two-signal technique. (b) Active loop technique.

For the two-signal technique (see Figure 3.13(a)), the input and output ports of the transistor are driven externally by the two signals from the power splitter. The power to the input port is controlled by the input variable attenuator and at the output port the magnitude and phase of the signal are controlled by varying an attenuator and a phase-shifter. The major problem in using this technique is that the load impedance is not constant with a varying input power.

In the active loop technique (see Figure 3.13(b)) the output power delivered by the device-under-test (DUT) is coupled, amplified, phase shifted, and, injected back to the DUT. The load impedance is controlled by varying the gain and phase-shift of the loop. By controlling the amplitude and phase of the injected signal, a wide range of impedances can be obtained. A narrow bandpass filter is added to avoid instabilities in the loop due to the relative broadband of the loop components. The benefit of using this technique, compared with the two-signal technique, is that, the load impedance is kept constant as long as the loop gain remains constant while varying the power level of the input signal generator [59].

The active loop technique can be extended to multi-harmonic load-pull [59]-[62], and, multi-harmonic load/source-pull [35], [63], since the loop is frequency selective.

More harmonic impedances can be tuned by adding an extra active loop for each harmonic. The measured results reported in [35], [59]-[63] have highlighted the important affect which harmonic tuning has on the efficiency of a PA, especially at the load second harmonic [59], [63], and, the source second harmonic [35], [63]. The effect of the first three source, and, load impedances for the active device, used in this thesis, is discussed in the following section.

3.5 Determination of Class-F PA Impedances Using a Novel Application of the Simulated Load/Source-Pull Method

In Chapter 2, on the assumption that the active device is modelled as a perfect lossless switch, analytical expressions were derived for the harmonic load impedances for maximum efficiency. Based on the simplified model of the device with linear transconductance, and, the effect of the parasitics included, expressions for the optimum load impedance for class-A and class-B PAs were derived [64]. Colantonia using the model of the device shown in Figure 3.1 and assuming the drain current is in the form of a truncated half-sinusoidal, general equations for the load impedances for a tuned-load and a class-F PA were derived [39]. In [65], the FET was modelled using static, small signal pulsed operating conditions and the effect of the second harmonic on the efficiency was investigated by exploiting the high-breakdown voltage of the device. However, in the design of high efficiency PAs, in order to ensure that practical and predicted results are in agreement it is necessary to use a full nonlinear non-unilateral model of the device. However, for the above models it is not possible to obtain analytical solutions for the optimum harmonic impedances so they are obtained using ADS software tool as discussed in this section.

In the ADS software tool, the FET is modelled as a full nonlinear equivalent circuit based on the Statz model and analysed using the HB method. The effect of the first three

harmonic impedances at the source and load, on efficiency, can be examined using the load/source-pull method. Impedance values and associated efficiencies are displayed on a Smith chart from which the impedance at maximum efficiency can be obtained. For this condition the drain voltage and current waveforms are checked for minimum overlap in time domain.

In the proposed design procedure [36], as the active device is non-unilateral, the effect on efficiency by the load and source impedance at each harmonic is investigated. The load/source-pull method which takes into account the nonlinearities and parasitics of the active device is presented. The advantage of using a simulation approach compared to the experimental-based systems discussed in the previous section is that the need for an expensive multi-harmonic load/source-pull experimental setup is avoided along with time consuming and potentially troublesome measurements.

In Figure 3.14, Z_{S1}, Z_{S2}, Z_{S3} are the source and Z_{L1}, Z_{L2}, Z_{L3} are the load impedances at the fundamental frequency, and second and third harmonics respectively.

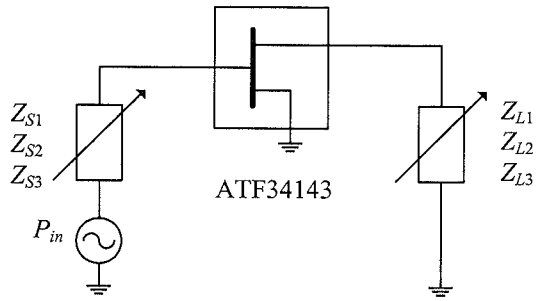


Figure 3.14: The simulated-based harmonic load/source-pull setup.

For a class-F PA design, the following ideal initial values, Z_{L2}=1 Ω, Z_{L3}=100 Ω, Z_{S2}=1 Ω, Z_{S3}=100 Ω are chosen for the second and third harmonics. For each simulation, the drain voltage, V_{ds} and current, I_{ds} waveforms were checked to ensure the area of overlap is minimised, and, the requirement for class-F PA fulfilled. Z_{S1} was optimised automatically at each simulation to achieve a conjugate match at the source terminal.

Simulation was carried out to sweep the values of Z_{L1}, Z_{L2}, Z_{L3}, Z_{S2}, and, Z_{S3} shown on the Smith chart in the following sub-sections.

The load/source-pull simulation steps are described below.

1. The load-pull method is applied to obtain an optimum value of Z_{L1} (Z^1_{L1}) for the above initial values of the second and third harmonic load and source impedances Z_{L2}, Z_{L3}, Z_{S2}, Z_{S3}.
2. Using the optimum value Z^1_{L1} the optimum value of Z_{S2} (Z^1_{S2}) is obtained from the source-pull. This is an essential step as this new impedance strongly affects the PAE. If there is a very small change in Z_{S2} between Steps 1 and 2, go to Step 5.
3. Z_{L1} is again optimised as in Step 1 to obtain Z^2_{L1}, using the value Z^1_{S2} found in Step 2.
4. Step 2 is repeated and a new value of Z_{S2} (Z^2_{S2}) is obtained to improve the PAE.
5. Using the new optimum values for Z_{L1} (Z^2_{L1}) and Z_{S2} (Z^2_{S2}), the load-pull is used to determine the optimum value of the second harmonic load impedance Z_{L2} (Z^1_{L2}). If little change in Z_{L2} between Step 5 and its initial value, go to Step 8.
6. Using the new value of Z_{L2} (Z^1_{L2}), a new optimum value of Z_{L1} (Z^3_{L1}) is obtained.
7. Step 5 is repeated and a new value of Z_{L2} (Z^2_{L2}) is obtained to improve the PAE.
8. Using the optimum values Z^3_{L1}, Z^2_{L2}, Z^2_{S2} load-pull is used to determine an optimum value of the third harmonic load impedance Z_{L3} (Z^1_{L3}).
9. Similarly, using the new optimum values, Z^3_{L1}, Z^2_{L2}, Z^2_{S2}, Z^1_{L3} the source-pull is used to determine the optimum value of the third harmonic source impedance Z_{S3} (Z^1_{S3}).

The above procedure has been applied to obtain the optimum load and source impedances for two class-F PAs operating at different frequencies, one operating at 0.9 GHz (Section 3.5.1) and the other one at 2.45 GHz (Section 3.5.2). For application in a mobile handset, a low V_{dd} of 3 V was applied. At 0.9 GHz, the active device was biased with a gate bias, V_{gg} of -0.7 V and an 8 dBm input power, P_{in} was used. At 2.45 GHz, the

active device was biased with a gate bias, V_{gg} of -0.5 V and was driven heavily into compression with a higher input power (P_{in}=13 dBm) for higher PAE. These applications are discussed in the following sub-sections.

3.5.1 The effect on the PAE of the first three harmonic load and source impedances at an operating frequency of 0.9 GHz

In this section an account of the steps used in the design approach for the PA is given.

Step 1: Determination of the first optimum value of Z^1_{L1}

Simulation was carried out to obtain Z_{L1} (Z^1_{L1}) for the second and third harmonic impedances using the given initial values. The centre of the load impedance sweep circle on the Smith chart was set to 50 Ω, the sweep circle radius set to 0.4, and 100 sweep points were set. Then 100 values for Z^1_{L1} were plotted on a Smith chart from which the first optimum value (highest PAE) for Z_{L1} (at marker) was selected for application in next step, as shown in Figure 3.15. A value of 64.1% was obtained for the PAE.

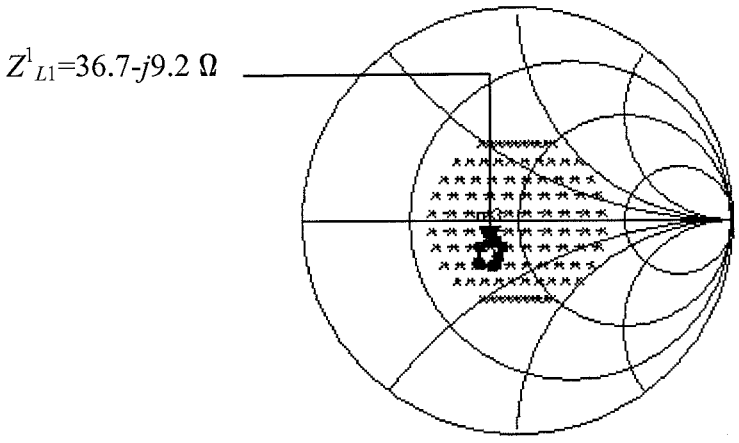


Figure 3.15: Load-pull on Z_{L1} at 0.9 GHz in Step 1.

The simulated drain voltage, V_{ds}, drain current, I_{ds}, and the gate voltage, V_{gs} waveforms corresponding to the value of Z_{L1} at marker are shown in Figure 3.16.

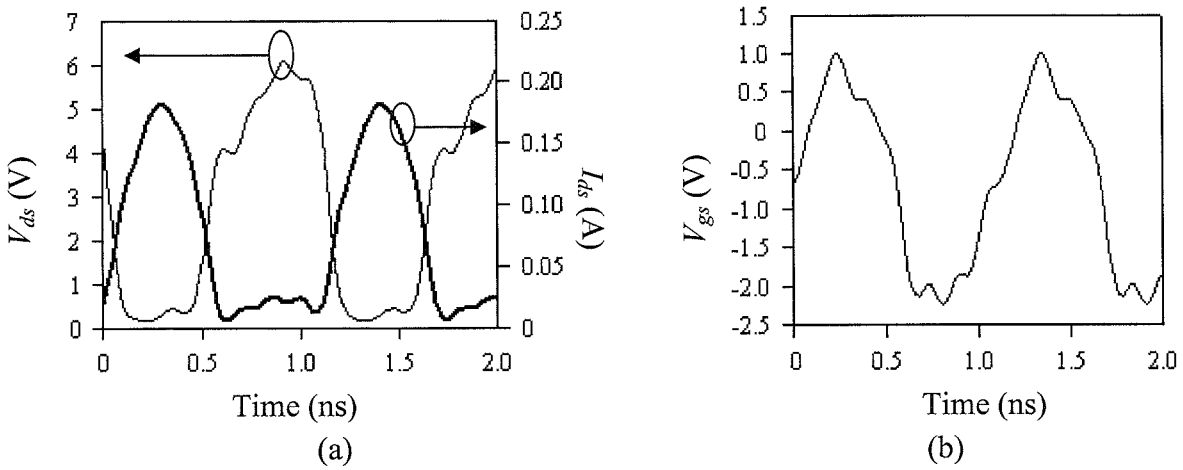


Figure 3.16: Simulated waveforms at 0.9 GHz in Step 1. (a) Drain. (b) Gate.

For the drain voltage/current waveforms, a square-like voltage waveform and a nearly half-sinusoidal current waveform were obtained, with the overlapping area of the drain voltage and current waveforms small. In Figure 3.16(b) a nearly symmetry (equally on-off duty cycle) gate voltage waveform was obtained indicating that the nonlinearity of the gate capacitance, C_{gs} is insignificant [66], [67].

Step 2: Determination of the first optimum value of Z^{1}_{S2}

The value Z^{1}_{L1} obtained in Step 1 is then used to obtain Z^{1}_{S2} with the other impedance values unchanged from their initial values. The centre of the impedance sweep circle was kept at 50 Ω. As the expected optimum value for Z_{S2} is small the radius of the sweep circle was specified as 0.95 and 100 values of Z_{S2} obtained. Figure 3.17 shows the locus for the optimum values for Z_{S2}, which produce a PAE of 64.6%.

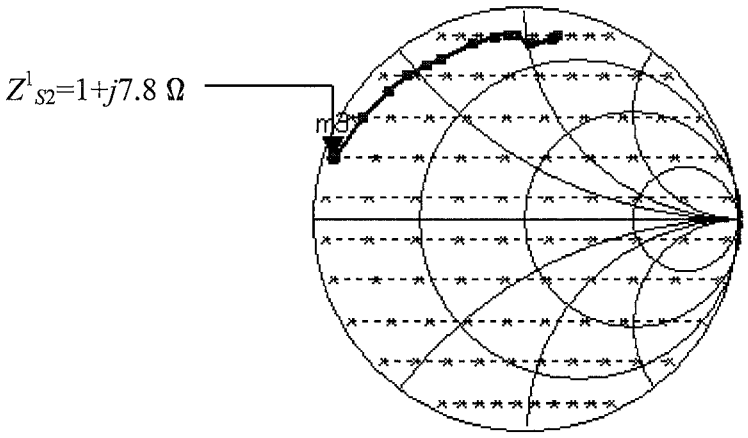
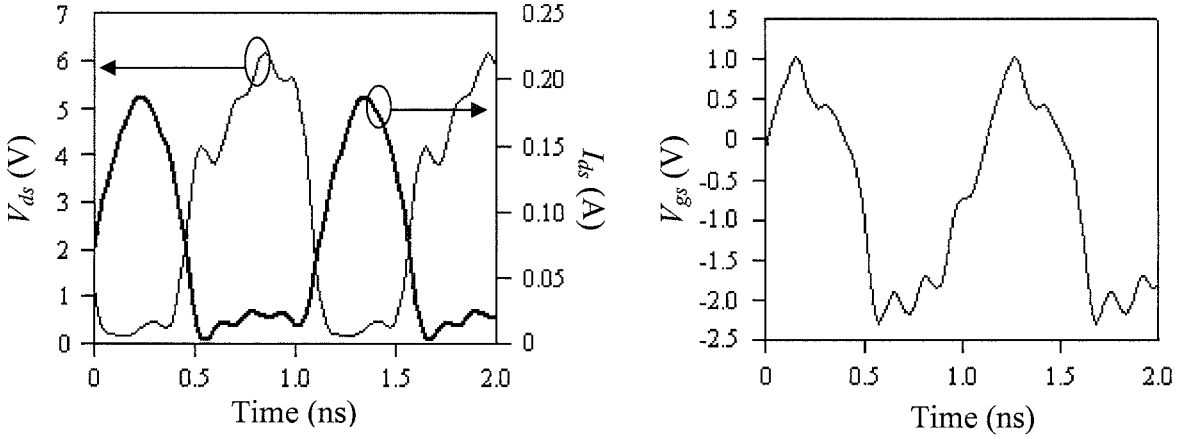


Figure 3.17: Source-pull on Z_{S2} at 0.9 GHz in Step 2.

From Figure 3.17 it can be seen that the locus for Z_{S2} is inductive and not zero, as predicted from the simple analysis (see Chapter 2), and, the real part is very small. As the lower inductance is little different from the ideal short circuit impedance (initial value) it is not necessary to repeat Steps 1 and 2 to improve the values for Z_{L1} and Z_{S2}, so Step 5 is next implemented. The simulated waveforms in Step 2 are shown in Figures 3.18.



(a) (b)

Figure 3.18: Simulated waveforms at 0.9 GHz in Step 2. (a) Drain. (b) Gate.

Step 5: Determination of the first optimum value of Z^{l}_{L2}

Using the optimum Z^{l}_{L1}, Z^{l}_{S2} from the Steps 1 and 2, simulation was carried out and the locus for the optimum second harmonic load impedance is shown in Figure 3.19.

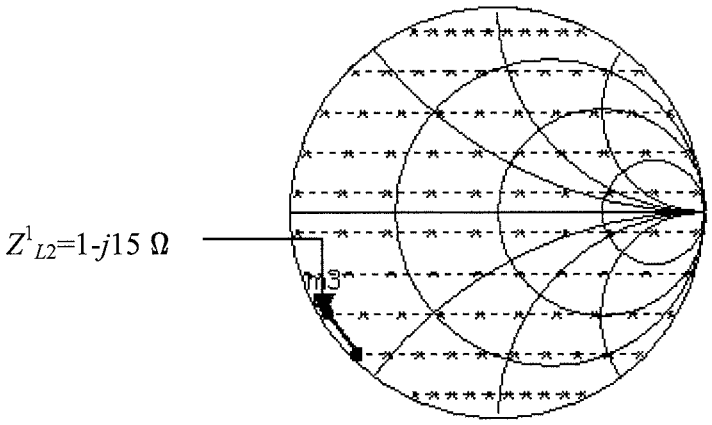
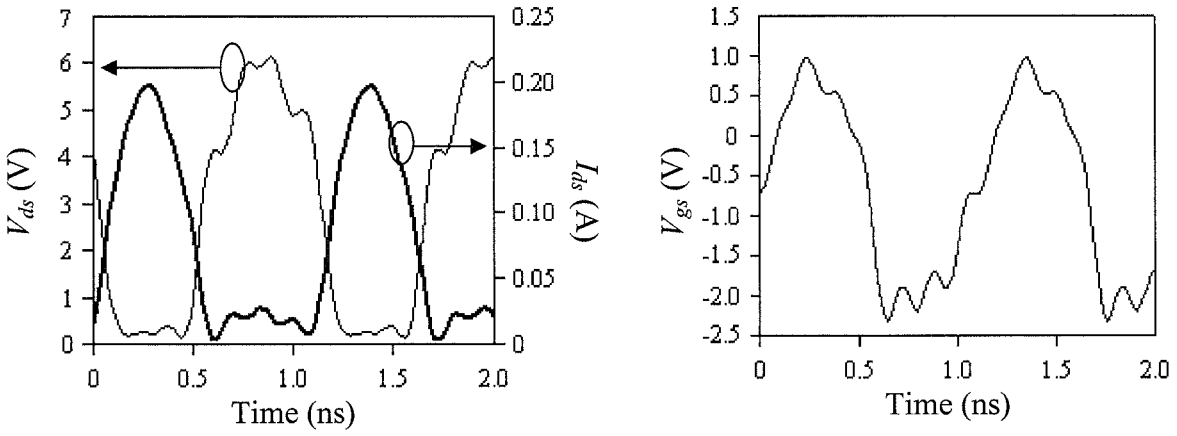


Figure 3.19: Load-pull on Z_{L2} at 0.9 GHz in Step 5.

A PAE of 68.2% was obtained, an improvement of 3.6%, compared with the short circuit termination for ideal class-F condition. The simulated waveforms are shown in Figure 3.20.



(a) (b)

Figure 3.20: Simulated waveforms at 0.9 GHz in Step 5. (a) Drain. (b) Gate.

Step 6: Re-optimisation of the value of Z_{L1}

Using the optimum values of Z^{1}_{S2}, Z^{1}_{L2} from the Steps 2 and 5, Z^{1}_{L1} was re-optimised For Z_{L1}, the centre of the sweep circle was set to the first optimal value of Z^{1}_{L1} and the sweep radius of the circle reduced to 0.3, using 100 impedance sweep points. The new

locus of Z^3_{L1} is shown in Figure 3.21 and a PAE of 68.4% was obtained. Simulated waveforms are shown in Figure 3.22.

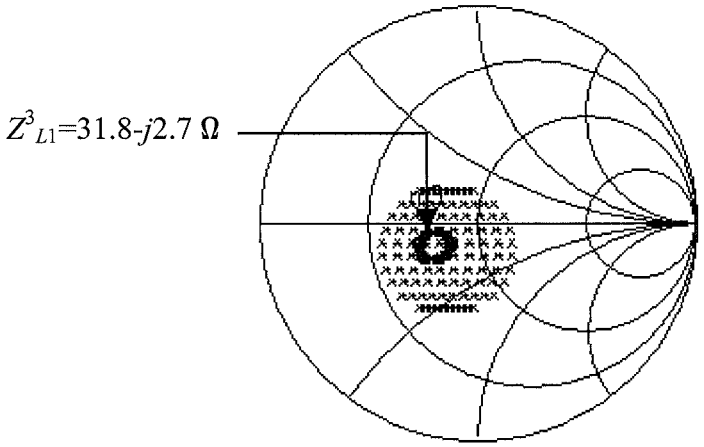
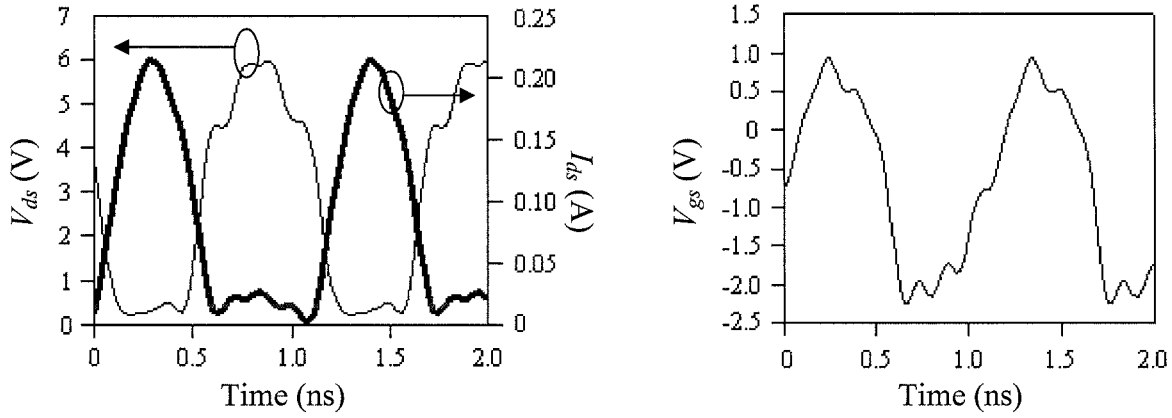


Figure 3.21: Load-pull on Z_{L1} at 0.9 GHz in Step 6.



(a) (b)

Figure 3.22: Simulated waveforms at 0.9 GHz in Step 6. (a) Drain. (b) Gate.

Step 7: Re-optimisation of the value of Z_{L2}

Similarly, with the optimum values of Z^1_{S2}, Z^3_{L1} from the Steps 2 and 6, Z^1_{L2} was re-optimised. For the new value Z^2_{L2} a PAE of 68.7% was obtained. The simulated waveforms are shown in Figure 3.24.

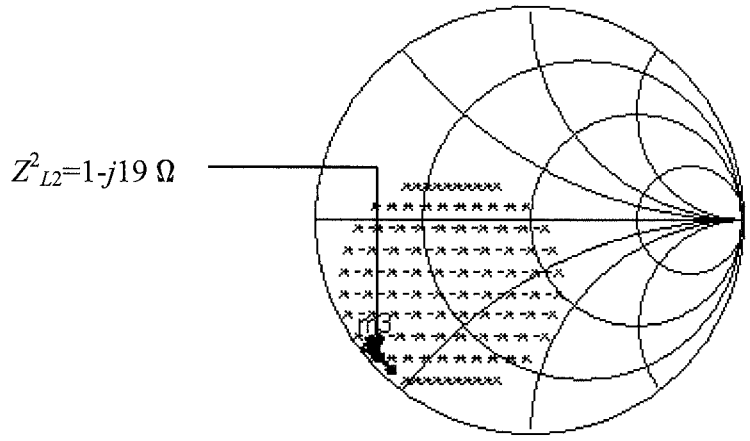
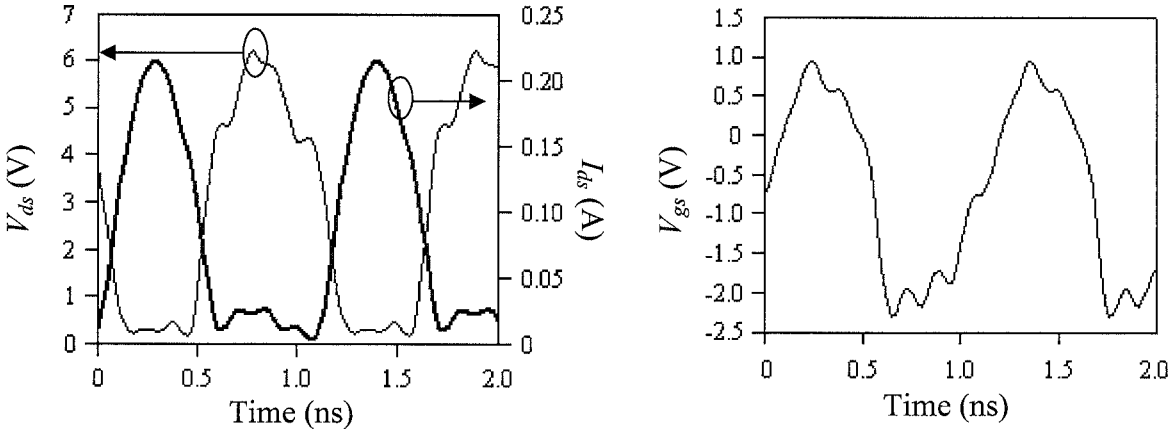


Figure 3.23: Load-pull on Z_{L2} at 0.9 GHz in Step 7.



(a) (b)

Figure 3.24: Simulated waveforms at 0.9 GHz in Step 7. (a) Drain. (b) Gate.

Step 8: Determination of the optimum value of Z^1_{L3}

The load-pull was carried out to obtain an optimum value of Z_{L3} using the optimum values of Z^3_{L1}, Z^2_{L2} and Z^1_{S2}. Figure 3.25 shows a locus of optimum values for Z^1_{L3}, for the PAE of 69.9%. The simulated waveforms are shown in Figure 3.26.

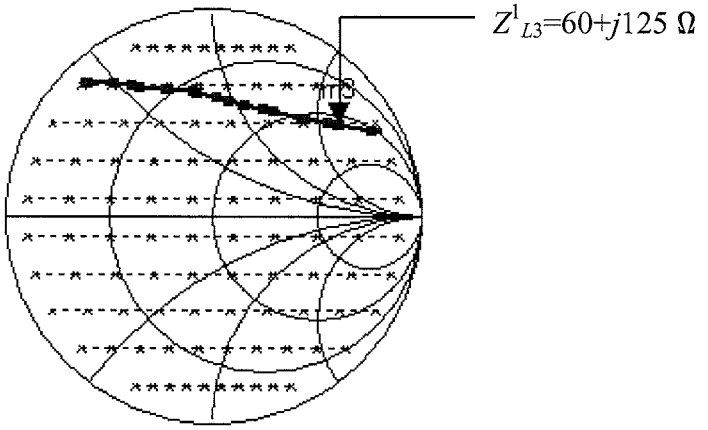
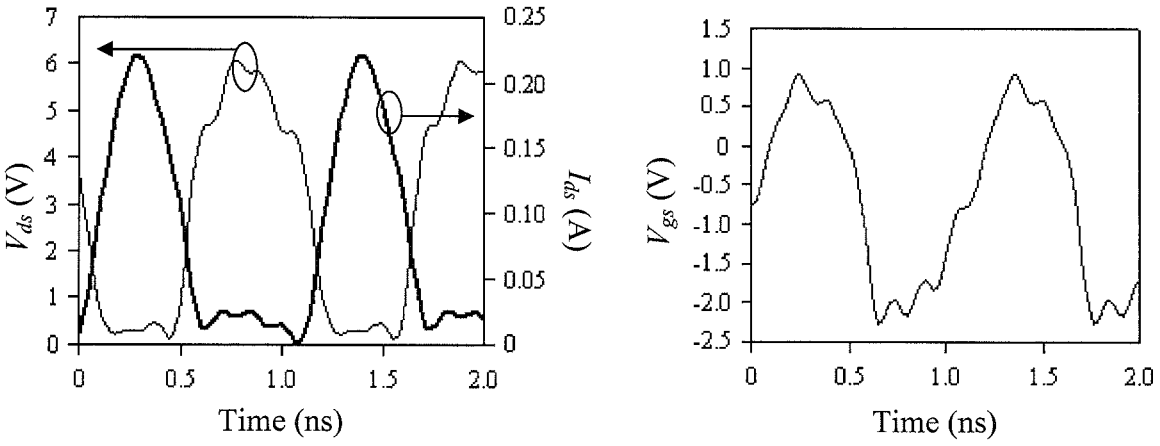


Figure 3.25: Load-pull on Z_{L3} at 0.9 GHz in Step 8.



(a) (b)

Figure 3.26: Simulated waveforms at 0.9 GHz in Step 8. (a) Drain. (b) Gate.

Step 9: Determination of the optimum value of Z^1_{S3}

Similarly, source-pull was carried out to obtain an optimum value of Z^1_{S3} using the optimum values Z^3_{L1}, Z^2_{L2}, Z^1_{S2}, and, Z^1_{L3}. A locus of optimum values for Z^1_{S3}, with a PAE of 70% is shown in Figure 3.27. The simulated waveforms are shown in Figure 3.28.

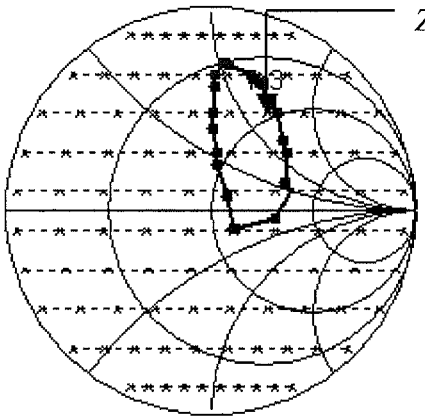
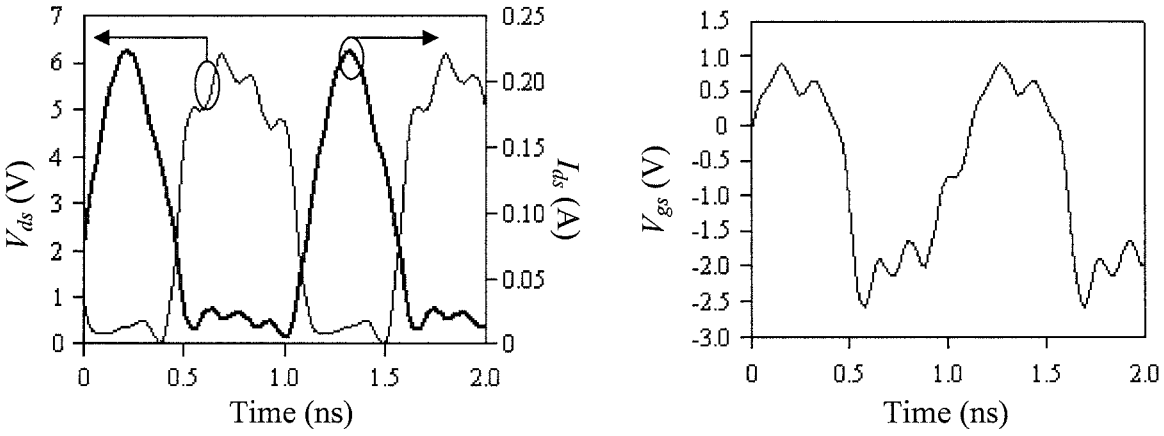


Figure 3.27: Source-pull on Z_{S3} at 0.9 GHz in Step 9.



(a) (b)

Figure 3.28: Simulated waveforms at 0.9 GHz in Step 9. (a) Drain. (b) Gate.

The optimum impedances and the PAE obtained in each step are summarised in Table 3.1 and the optimum impedances obtained at 0.9 GHz are given in Table 3.2.

Step	Optimised impedance (Ω)	PAE (%)
1	Z^1_{L1}=36.7-j9.2	64.1
2	Z^1_{S2}=1+j7.8	64.6
5	Z^1_{L2}=1-j15	68.2
6	Z^3_{L1}=31.8-j2.7	68.4
7	Z^2_{L2}=1-j19	68.7
8	Z^1_{L3}=60+j125	69.9
9	Z^1_{S3}=47+j68	70.0

Table 3.1: Optimum impedances and the PAEs obtained in each step.

Harmonic	Source impedance, $Z_S(\Omega)$	Load impedance, $Z_L(\Omega)$
1	31+*j*136	31.8-*j*2.7
2	1.3+*j*7.8	1-*j*19
3	47+*j*68	60+*j*125

Table 3.2: Simulated optimum Z_S and Z_L obtained at 0.9 GHz.

It is noted that the above load and source impedances obtained are not purely resistive which is due to the nonlinearity and the packaged parasitics which exist in the actual active device. The PA performance is hugely affected if the parasitic reactance is not taken into account. From the simulated results, the PAE is less affected by the source second and third harmonic impedances compared to the load impedances. Also, the source third harmonic impedance has the least influence on the PAE.

3.5.2 The effect on the PAE of the first three harmonic load and source impedances at an operating frequency of 2.45 GHz

The Smith chart and waveforms, for each step are given below.

Step 1: Determination of the first optimum value of Z^1_{L1}

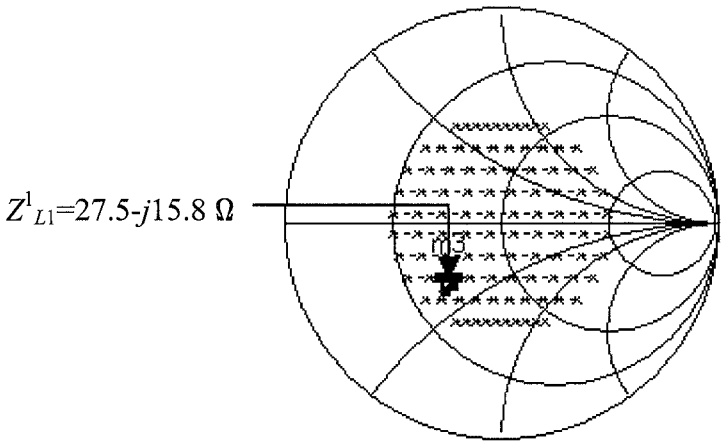


Figure 3.29: Load-pull on Z_{L1} at 2.45 GHz in Step 1.

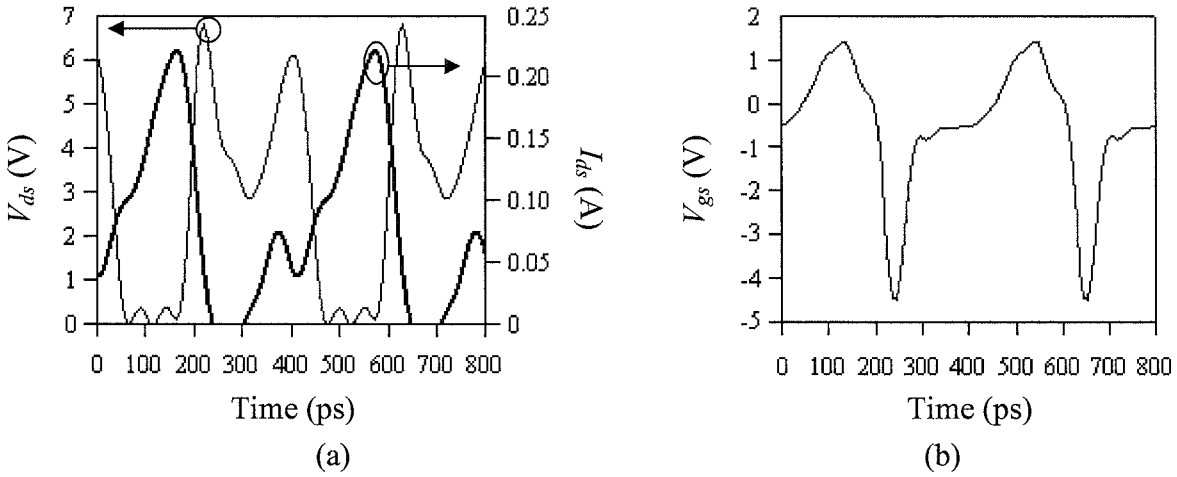


Figure 3.30: Simulated waveforms at 2.45 GHz in Step 1. (a) Drain. (b) Gate.

In Figure 3.30(b) a deep negative spike, (longer turn-on cycle) gate voltage waveform was obtained for the initial value of Z_{S2}=1 Ω. The strong negative spike is mainly caused by the nonlinearity of the gate capacitance, C_{gs} [66], [67], in contrast to the result obtained for an operating frequency of 0.9 GHz where gate voltage falls to only about -2.5 V. This effect is reflected in the resultant drain voltage/current waveforms, shown in Figure 3.30(a). With the distorted/unequal input signal, the drain current/voltage waveforms are significantly different from the ideal half-sinusoidal and square waveforms, resulting in huge power dissipation in the active device. A PAE of 37.8% was obtained.

Step 2: Determination of the first optimum value of Z^{1}_{S2}

To compensate for the nonlinearity of the gate capacitance, C_{gs}, the application of source-pull on Z_{S2} is an essential step.

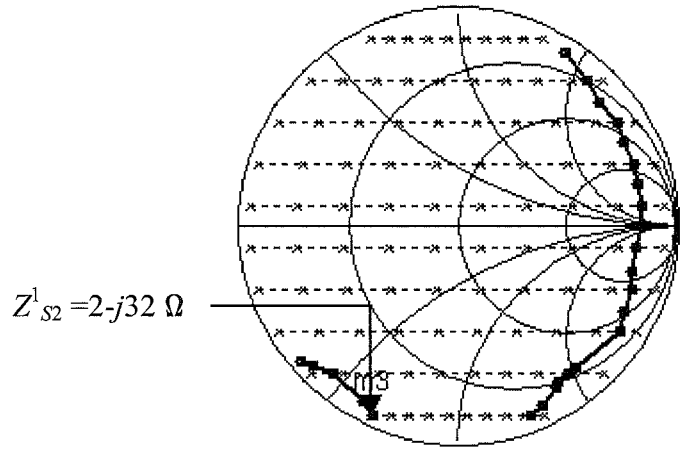
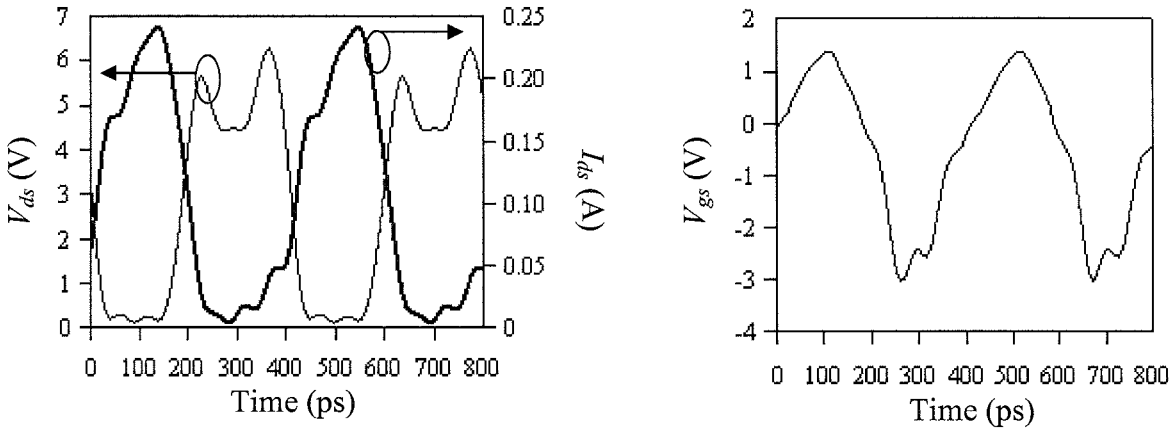


Figure 3.31: Source-pull on Z_{S2} at 2.45 GHz in Step 2



(a) (b)

Figure 3.32: Simulated waveforms at 2.45 GHz in Step 2. (a) Drain. (b) Gate.

As can be seen (Figure 3.32(b)), the strong negative spike occurred in Figure 3.30(b) has disappeared and a nearly symmetry (equally on-off duty cycle) gate voltage was obtained for the optimum value of Z_{S2}. Also, for the drain current/voltage waveforms (see Figure 3.32(a)), the overlapping area between the drain voltage and current waveforms is small, therefore the power dissipated in the active device is also be small, and, the PAE is increased to 59.3%.

Step 3: Re-optimisation of the value of Z_{L1}

The new locus of Z^2_{L1} is shown in Figure 3.33 and an increment of 4% PAE was obtained.

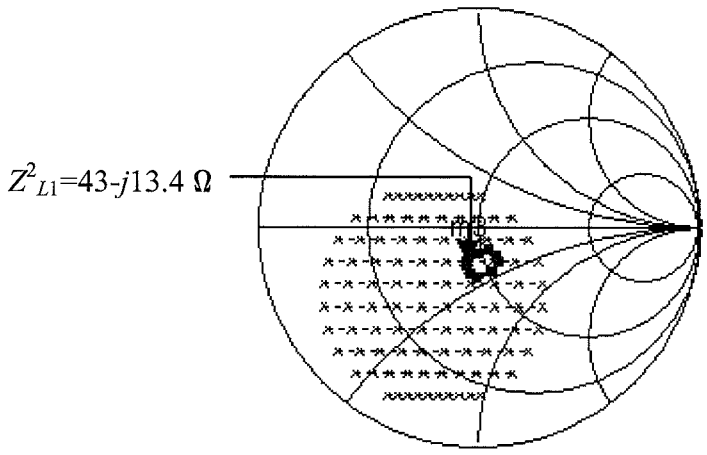
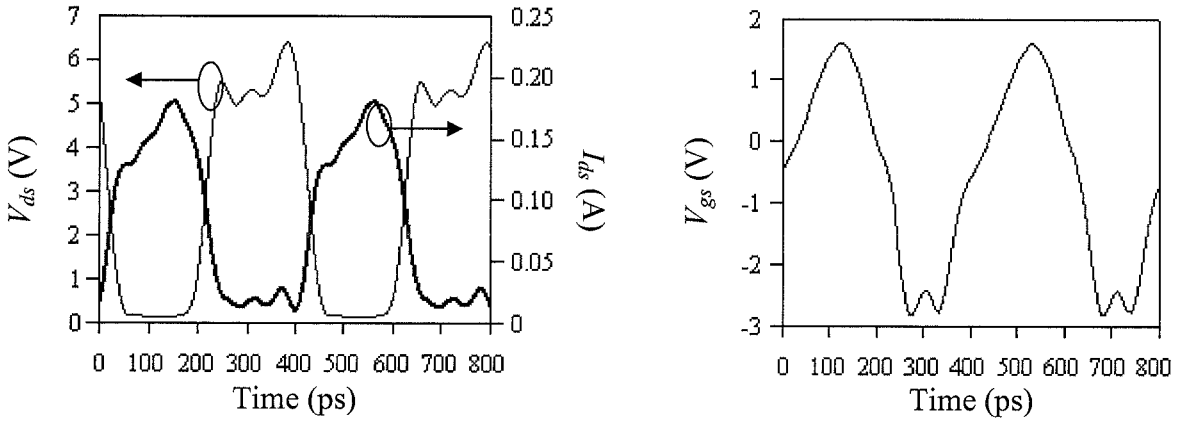


Figure 3.33: Load-pull on Z_{L1} at 2.45 GHz in Step 3.



(a) (b)

Figure 3.34: Simulated waveforms at 2.45 GHz in Step 3. (a) Drain. (b) Gate.

Step 4: Re-optimisation of the value of Z_{S2}

The new locus of Z^2_{S2} is shown in Figure 3.35 and an increment of 0.5% PAE was obtained.

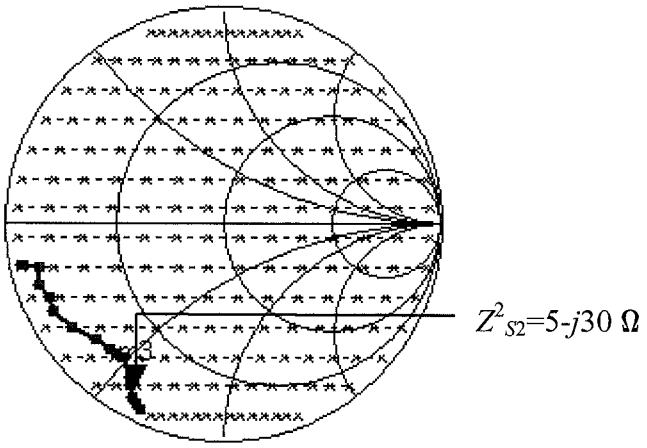
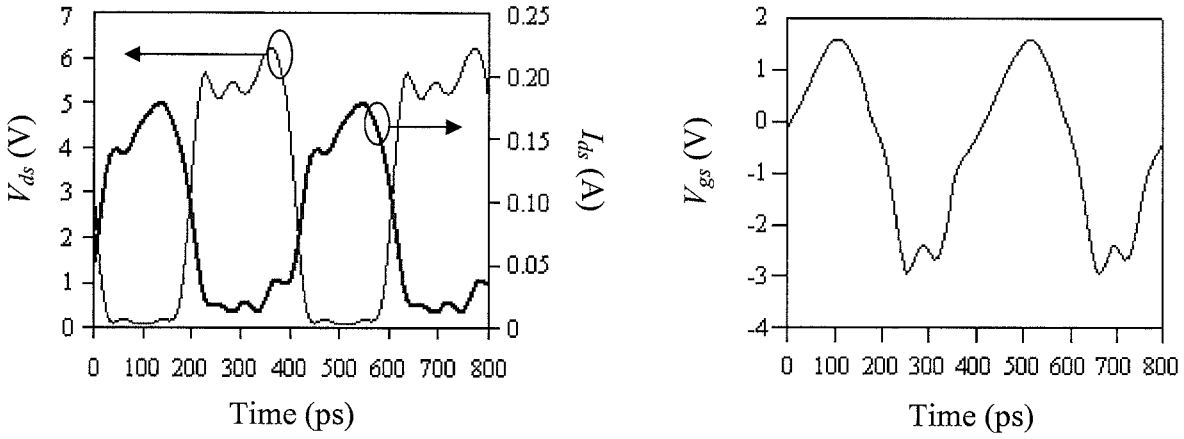


Figure 3.35: Source-pull on Z_{S2} at 2.45 GHz in Step 4.



(a) (b)

Figure 3.36: Simulated waveforms at 2.45 GHz in Step 4. (a) Drain. (b) Gate.

Step 5: Determination of the first optimum value of Z^1_{L2}

A PAE of 69.8% was obtained this being an improvement of 6% compared with the short circuit termination for the ideal class-F condition.

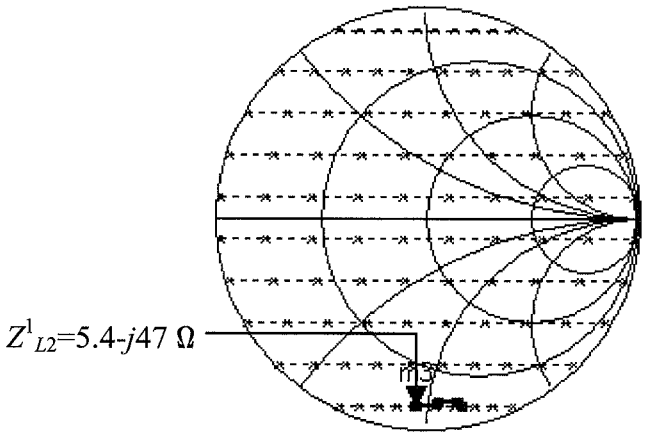
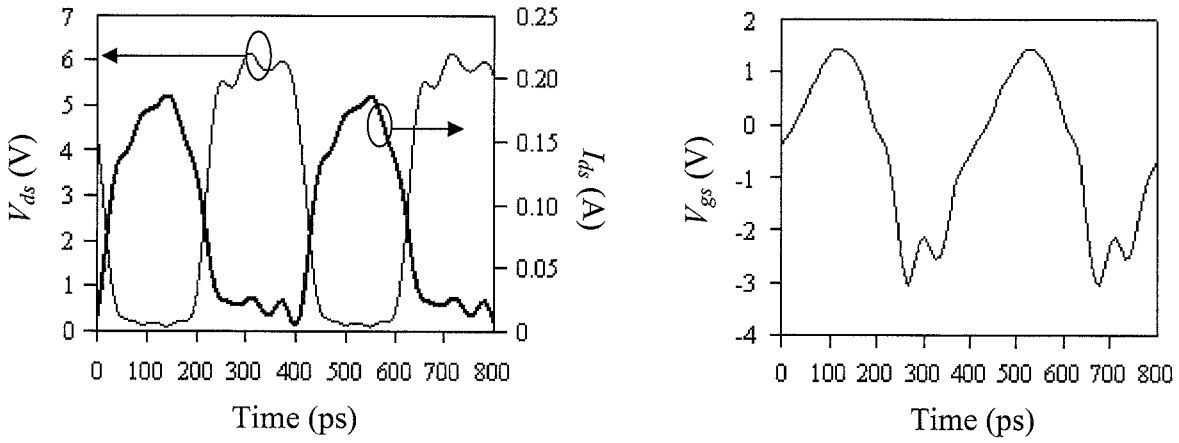


Figure 3.37: Load-pull on Z_{L2} at 2.45 GHz in Step 5.



(a) (b)

Figure 3.38: Simulated waveforms at 2.45 GHz in Step 5. (a) Drain. (b) Gate.

Step 6: Re-optimisation of the value of Z_{L1}

The new locus of Z^3_{L1} is shown in Figure 3.39 and an improvement of 0.5% PAE was obtained.

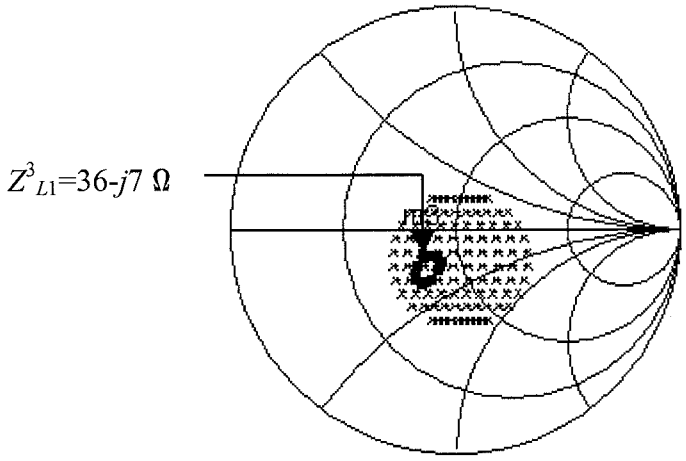
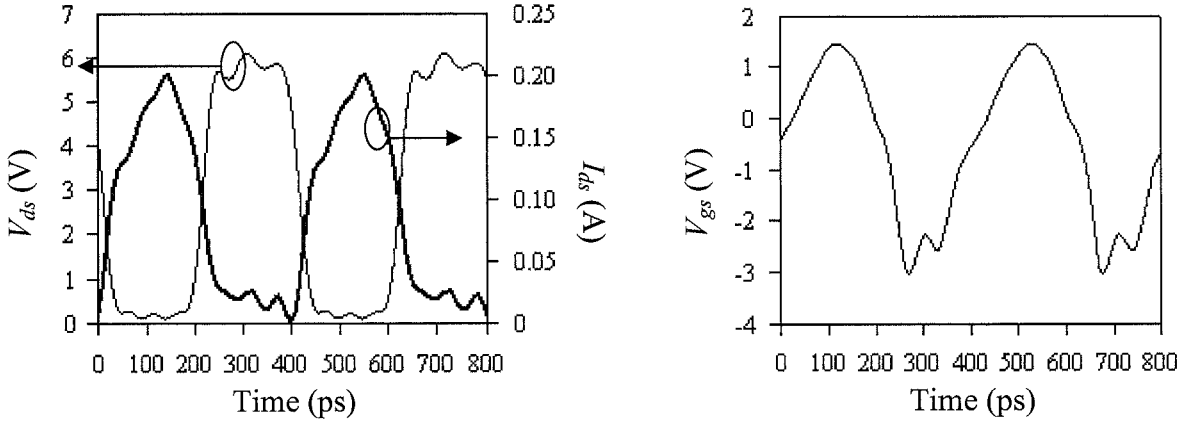


Figure 3.39: Load-pull on Z_{L1} at 2.45 GHz in Step 6.



(a) (b)

Figure 3.40: Simulated waveforms at 2.45 GHz in Step 6. (a) Drain. (b) Gate.

Step 7: Re-optimisation of the value of Z_{L2}

The new locus of Z^2_{L2} is shown in Figure 3.41 and an improvement of 0.6% PAE was obtained.

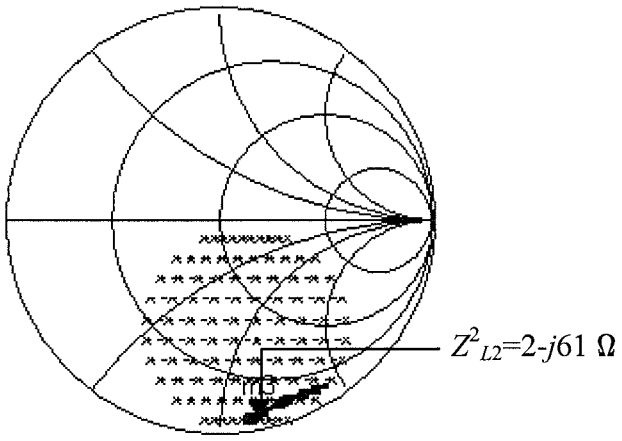
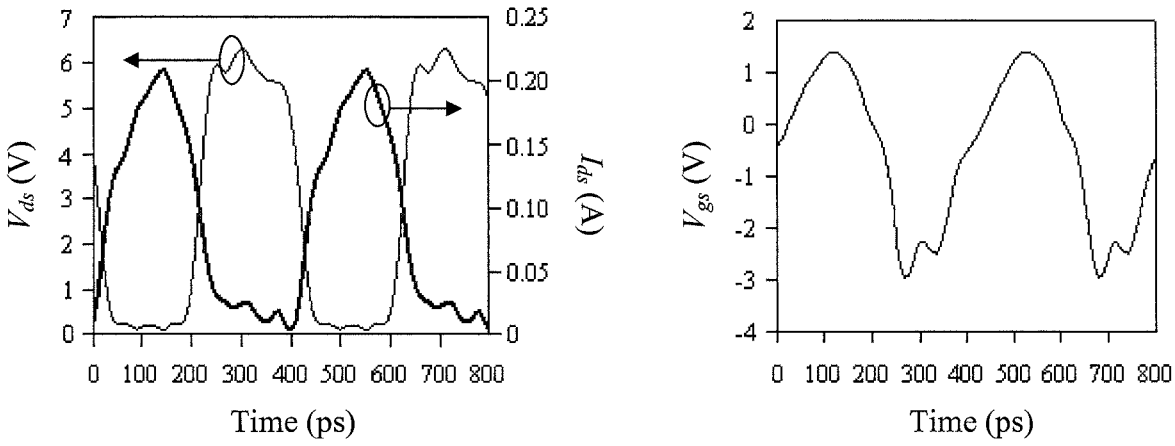


Figure 3.41: Load-pull on Z_{L2} at 2.45 GHz in Step 7.



(a) (b)

Figure 3.42: Simulated waveforms at 2.45 GHz in Step 7. (a) Drain. (b) Gate.

Step 8: Determination of the optimum value of Z^1_{L3}

A PAE of 73.9% was obtained with an improvement of 3% compared with the initial value of Z_{L3}.

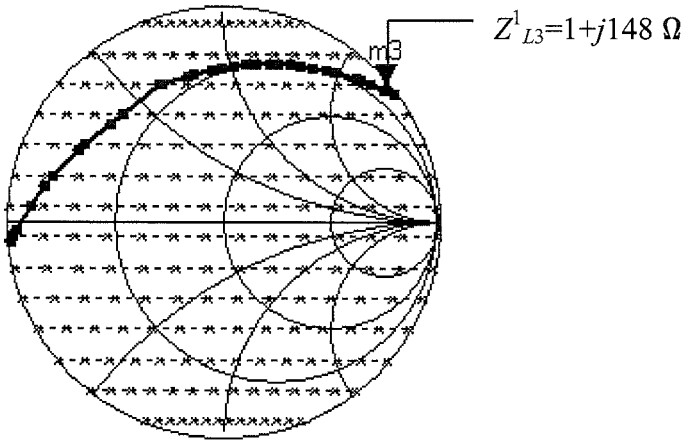
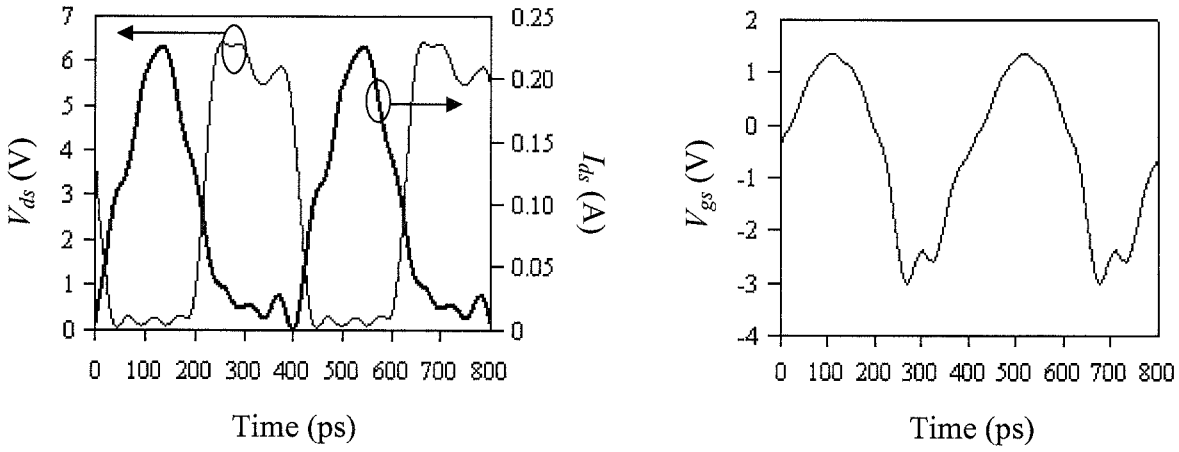


Figure 3.43: Load-pull on Z_{L3} at 2.45 GHz in Step 8.



(a) (b)

Figure 3.44: Simulated waveforms at 2.45 GHz in Step 8. (a) Drain. (b) Gate.

Step 9: Determination of the optimum value of Z^1_{S3}

A PAE of 74.3% was obtained with an improvement of 0.4% compared with the initial value of Z_{S3}.

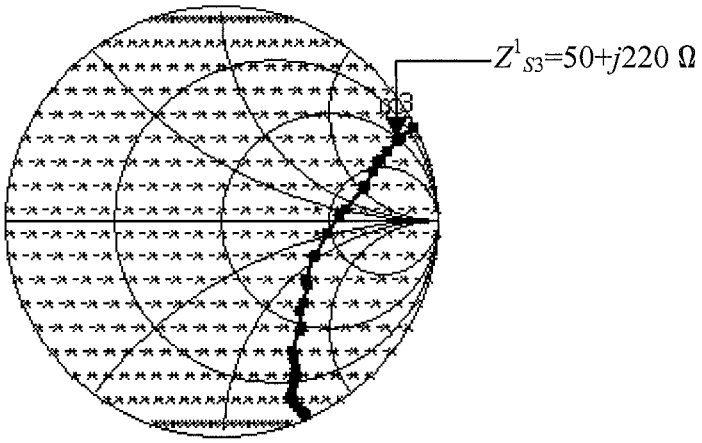
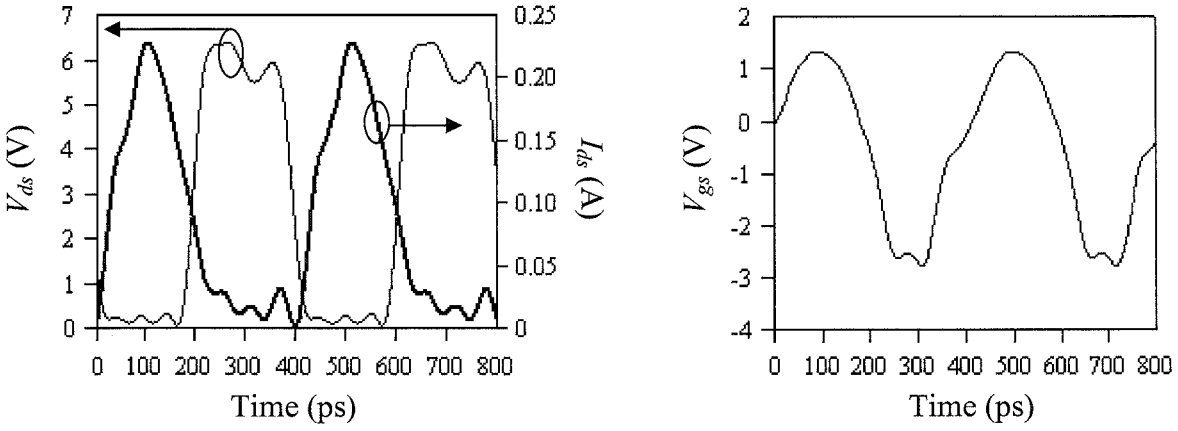


Figure 3.45: Source-pull on Z_{S3} at 2.45 GHz in Step9.



(a) (b)

Figure 3.46: Simulated waveforms at 2.45 GHz in Step 9. (a) Drain. (b) Gate.

The optimum impedances and the PAE obtained in each step are summarised in Table 3.3 and the optimum impedances obtained at 2.45 GHz are given in Table 3.4.

Step	Optimised impedance (Ω)	PAE (%)
1	Z^1_{L1}=27.5-j15.8	37.8
2	Z^1_{S2} =2-j32	59.3
3	Z^2_{L1}=43-j13.4	63.3
4	Z^2_{S2}=5-j30	63.8
5	Z^1_{L2}=5.4-j47	69.8
6	Z^3_{L1}=36-j7	70.3
7	Z^2_{L2}=2-j61	70.9
8	Z^1_{L3}=1+j148	73.9
9	Z^1_{S3}=50+j220	74.3

Table 3.3: Optimum impedances and the PAEs obtained in each step.

Harmonic	Source impedance, $Z_S(\Omega)$	Load impedance, $Z_L(\Omega)$
1	17+*j*28	36-*j*7
2	5-*j*30	2-*j*61
3	50+*j*220	1+*j*148

Table 3.4: Simulated optimum Z_S and Z_L obtained at 2.45 GHz.

It is noted that at 2.45 GHz, the parasitic reactance is higher than the value obtained for an operating frequency of 0.9 GHz. The PA performance is hugely affected if the parasitic reactance is not taken into account, especially at the source and load second harmonic impedances. The PAE is less affected by the load and source third harmonic impedances compared to the source second harmonic, and the load fundamental frequency and second harmonic impedances.

3.5.3 The effect on the PAE of the source second harmonic, and, the load first and second harmonic impedances over the frequency range 2.15-2.75 GHz

The most critical impedance components affecting the PAE are the source second harmonic and, the load fundamental frequency and second harmonic, so only these impedances were examined. In this section optimum impedances for these components at seven frequencies over the range 2.15-2.75 GHz are obtained.

Figures 3.47, 3.48 and 3.49 show how the PAE varies with the Z_{L1}, Z_{L2} and Z_{S2} over a wide range of frequency. PAE contours were plotted at the seven frequency points 2.15 GHz, 2.25 GHz, 2.35 GHz, 2.45 GHz, 2.55 GHz, 2.65 GHz and 2.75 GHz. The plots divide into three regions which include the optimum region, the region where the PAE is above or equal to 60%, and, the region below 60%.

At the fundamental load impedance, Z_{L1}, the optimum impedances in the frequency range from 2.15-2.75 GHz, remains at the same location on the Smith chart (see Figure 3.47). It is also noticed that the region where the PAE is above or equal to 60% is constant. Hence, the active device can be matched over a wide frequency range.

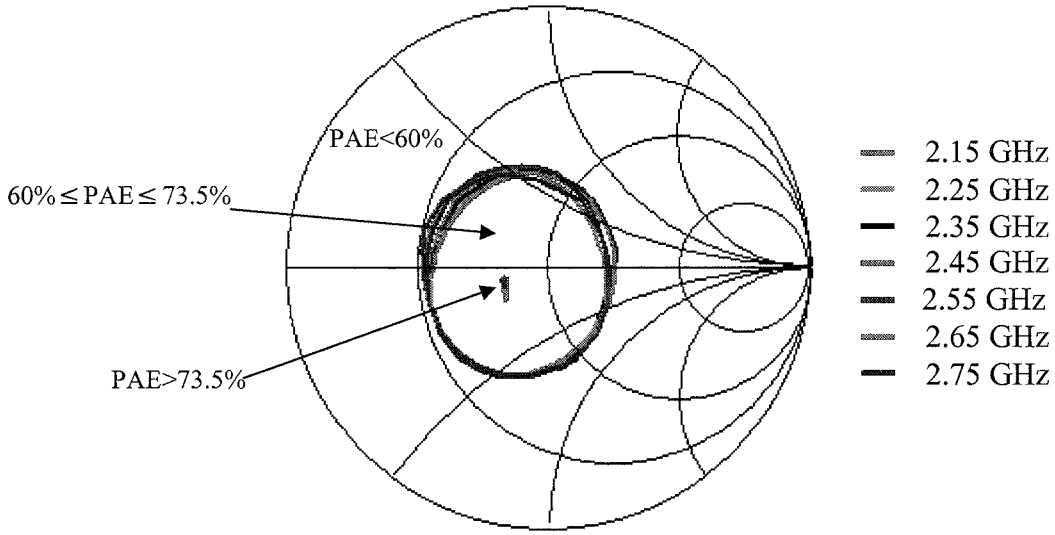


Figure 3.47: PAE plotting against Z_{L1} at different frequency points.

At the second harmonic, the set of optimum load impedances, Z_{L2}, are capacitive reactances (see Figure 3.48). The capacitance increases with frequency. In the higher frequency range 2.55-2.75 GHz the PAE drops faster to below 60% as compared to the drop in the lower range 2.15-2.45 GHz.

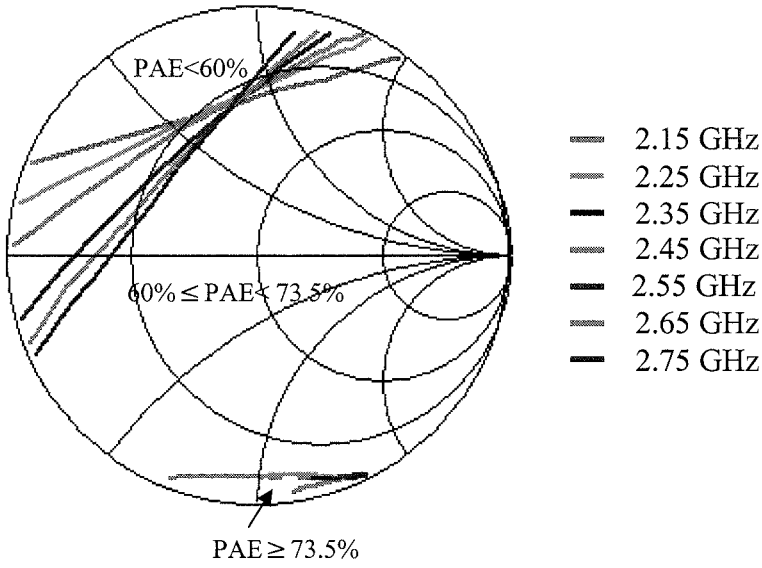


Figure 3.48: PAE plotting against Z_{L2} at different frequency points.

In Figure 3.49 the optimum value of the Z_{S2} at 2.15 GHz is less capacitive compared with the value at higher frequency points. Again, Z_{S2} at 2.75 GHz is most capacitive, this being due to the increase in parasitic reactance with frequency. The region ($60\% \leq PAE \leq 75.5\%$) for the source impedance is smaller compared with that of the load impedance. The PAE drops faster below 60% in the higher frequency range.

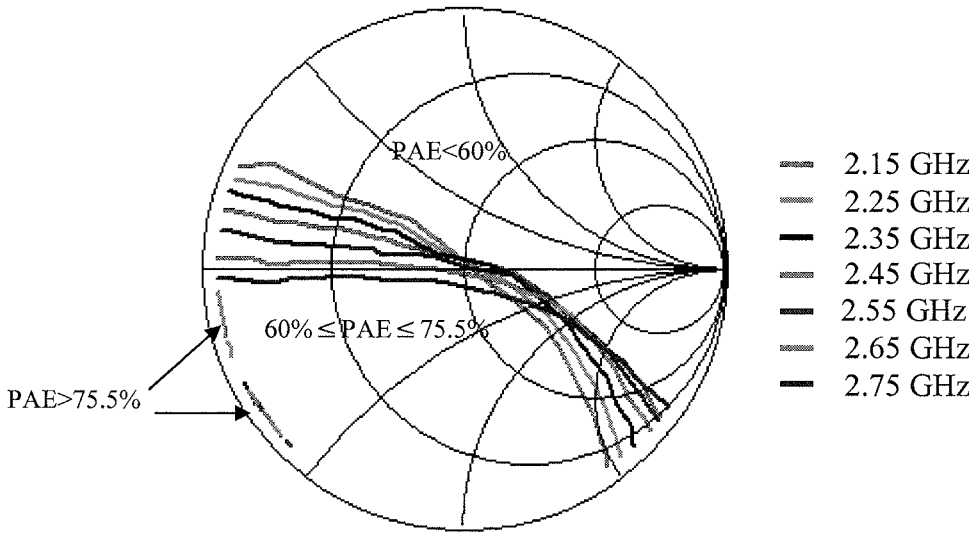


Figure 3.49: PAE plotting against Z_{S2} at different frequency points.

3.6 Summary

A review of nonlinear modelling, and, load/source-pull method has been discussed along with the stability conditions for the active device. The results obtained from simulation have been presented.

A novel application of the simulated load/source-pull method to obtain the optimum load and source impedances for two class-F PAs operating at 0.9 GHz and 2.45 GHz is presented, and, the effect of the fundamental frequency, and second and third harmonic impedances on the PAE are discussed. Simulated results show that the values of Z_{L1}, Z_{L2} and Z_{S2} have a significant effect on the PAE as compared with the values of Z_{L3} and Z_{S3}. The results also showed that the effect of the harmonic impedances on the PAE is more

critical at 2.45 GHz than at 0.9 GHz. At 2.45 GHz, from amongst the harmonic impedances, Z_{L2}, Z_{S2}, Z_{L3}, Z_{S3}, the source second harmonic, Z_{S2} has the strongest effect on the PAE. This is because the parasitic reactances increase with frequency.

Very useful information for a broad bandwidth high efficiency PA design has also been obtained using the load/source-pull method. The fundamental load, Z_{L1} is the essential key parameter in achieving a high PAE over a wide bandwidth. However, the overall PAE bandwidth will degrade if the source and load second harmonic impedances, Z_{L2} and Z_{S2} are terminated with a wrong amplitude and phase while the overall PAE bandwidth will improve if the source and load second harmonic impedances, Z_{L2} and Z_{S2} are terminated with a correct amplitude and phase. In order to design a broad bandwidth high efficiency PA, the load impedances, Z_{L1}, Z_{L2} together with the source impedance, Z_{S2}, need to achieve optimal values over a complete range of frequencies.

To verify the results obtained by simulation, class-F PA circuits operating at 0.9 GHz and 2.45 GHz were fabricated. Matching circuits were designed to provide the desired impedances to the active device at the first two harmonics and the first three harmonics at the source and load terminals. This is discussed in Chapters 4 and 5.

CHAPTER 4 DESIGN OF A HIGH EFFICIENCY CLASS-F POWER AMPLIFIER OPERATING AT 0.9 GHZ

4.1 Introduction

In this chapter a new proposed load harmonic matching network is designed so that the active device is terminated by the optimum impedances obtained in Chapter 3. Based on these designs the PA was fabricated and measured values of the output power, power gain and PAE, were obtained. It is shown that there is a very good agreement between the measured and simulated results.

In Section 4.2 a review is presented of the different forms of the load matching networks and the efficiencies reported in published papers. Details of the source matching network and the new proposed load harmonic matching network are discussed in Section 4.3. For the load a two-lumped-element L-C matching network is used to obtain the required load impedances at the fundamental frequency and the third harmonic. The lumped elements are replaced by two transmission lines as this greatly simplifies the practical realisation of the circuit. Another transmission line is used in this network to obtain the required impedance at the second harmonic. To increase the conjugate match bandwidth at the source terminal for the fundamental frequency a three-element T-network is used. Based on these designs the PA was fabricated and the results obtained are discussed in Section 4.4. In Section 4.5 the measured PAE of 71.4% obtained by this PA is compared with those reported in literature. Based on this work two papers have been published in [68] and [69].

4.2 Literature Survey of the Load Matching Networks for Class-F PAs

In the case of an ideal class-F PA, where the active device acts as a switch, maximum efficiency is obtained by loads which have short circuits at the even harmonics

and open circuits at the odd harmonics. Chiba [70] used a $\lambda/4@2f_1$ open circuit stub connected in parallel with a series microstrip line to obtain short circuits at the even harmonics. Lin [71] used a $\lambda/4@f_1$ short circuit stub to produce a short circuit at the second harmonic. In order to compensate for the effects of active device parasitics, Nojima [72] used a trimmer capacitor to obtain a short circuit at the second harmonic. The odd harmonic impedances were not considered in any of the above designs [70]-[72]. To reduce the size of a class-F PA, Toyoda [73] used dielectric resonators to implement classical Tyler-type third- and fifth- harmonic output networks. Huang [74], Duvanaud [75], Grebennikov [76], and, Ko [77] designed the output network to obtain a short circuit at the second harmonic by using a $\lambda/4@f_1$ microstrip line. To obtain the required high impedance at the third harmonic a $\lambda/4@3f_1$ open circuit stub was connected in parallel with a series microstrip line. Wren [78] used Rhodes's low-pass matching network topology [79] to produce the required impedances up to the third harmonic. Recently, in order to reduce the size of the PA, Aikawa [80] has successfully realised a lumped-element circuit design to obtain the required impedances up to the fourth harmonic. The latest class-F PA using a lumped-element circuit was successful in achieving the required impedances up to the seventh harmonic [81]. However, these circuit topologies become more and more complicated and also increase the circuit losses especially at higher frequencies thereby reducing efficiency.

4.3 Design of Load and Source Matching Networks for a Class-F PA Operating at 0.9 GHz

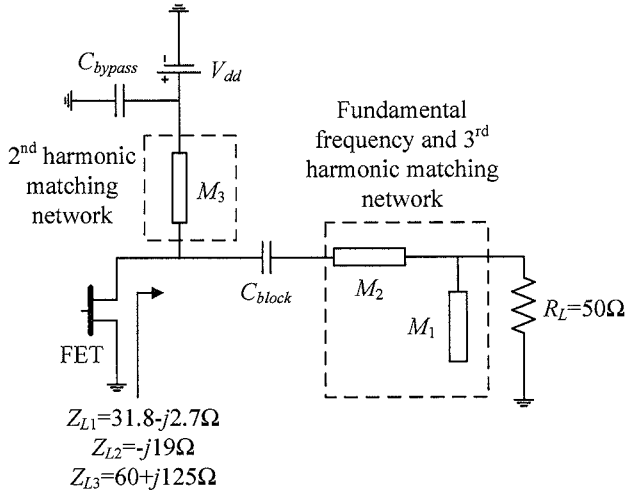
In Chapter 3 the optimum harmonic load and source impedances of the active device for maximum efficiency, at the operating frequency 0.9 GHz, were obtained. For the load, the impedances at the fundamental frequency, the second, and, third harmonics are Z_{L1}=31.8-j2.7 Ω, Z_{L2}=1-j19 Ω and Z_{L3}=60+j125 Ω, and, the source impedances were

Z_{S1}=31+j136 Ω, Z_{S2}=1.3+j7.8 Ω and Z_{S3}=47+j68 Ω. As found in Chapter 3 only a conjugate match for the source at the fundamental frequency was required.

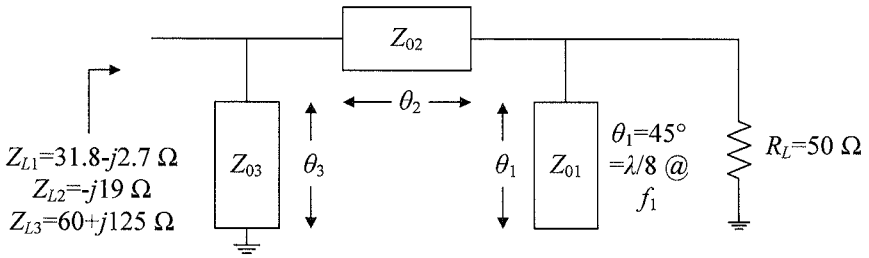
4.3.1 New proposed load matching network for the first three harmonics

To obtain the required impedance Z_{L1} at the fundamental frequency, a two-lumped-element L-C matching network was first designed. The lumped elements were then replaced by a high impedance series line and an open circuit stub of length $\lambda/4@2f_1$. As this stub produces a short circuit at the second harmonic it is then possible to independently obtain the desired impedance Z_{L2} at the second harmonic. The approximate value for the third harmonic load impedance Z_{L3} is obtained by fine tuning this network.

The new proposed network is shown in Figures 4.1(a) and (b), where, Z_{01}, Z_{02}, Z_{03} are the characteristic impedances and θ_1, θ_2, θ_3 are the electrical lengths of the transmission lines, M_1, M_2, M_3.



(a)



(b)

Figure 4.1: (a) Load matching network. (b) AC equivalent circuit.

The two-lumped-element L-C matching network used to transform the 50 Ω to the impedance Z_{L1} is shown in Figure 4.2. The details of the design of this network are given in *Appendix 4A* [82].

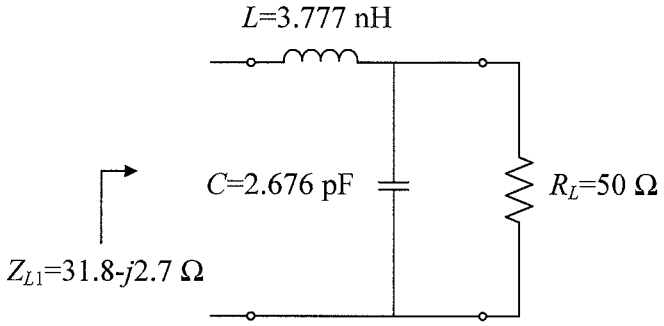


Figure 4.2: Two-lumped-element L-C matching network.

The lumped circuit elements L, C were realised using transmission lines (see Figure 4.3). The shunt capacitor was realised by an open circuit stub, and, the inductor was realised by a short length transmission line of high characteristic impedance.

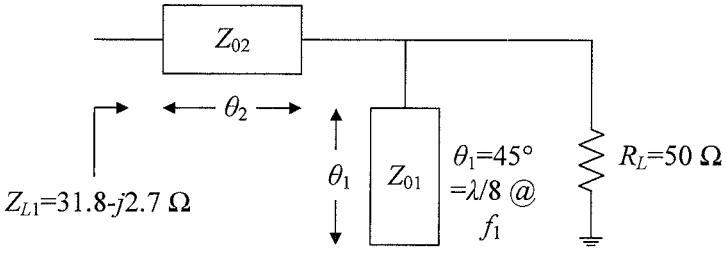


Figure 4.3: Transmission line matching network.

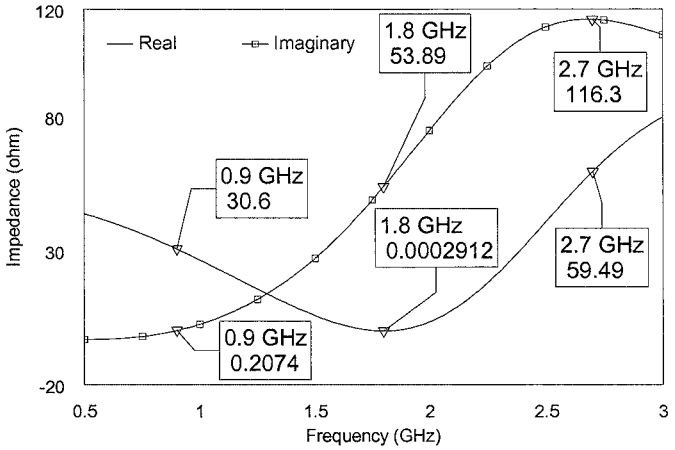


Figure 4.5: Simulated impedance response of the transmission line matching network after fine tuned θ_2.

The small effect on the imaginary part of Z_{L1} by the change in the length of θ_2 can be reduced by using a suitable value of the capacitor C_{block} (see Figure 4.1(a)).

In Figure 4.1, in order to produce a short circuit at the junction of the two lines M_1 and M_2 at the second harmonic, the electrical length θ_1 is chosen to be $\lambda/8@f_1$. As a result this isolates the load resistor R_L and causes the lines M_2, M_3 to be in parallel. It is now possible to use equation (4.1) to calculate the electrical length θ_3 so that the active device is terminated by the optimum impedance of Z_{L2} ($-j19\ \Omega$) (see Figure 4.6).

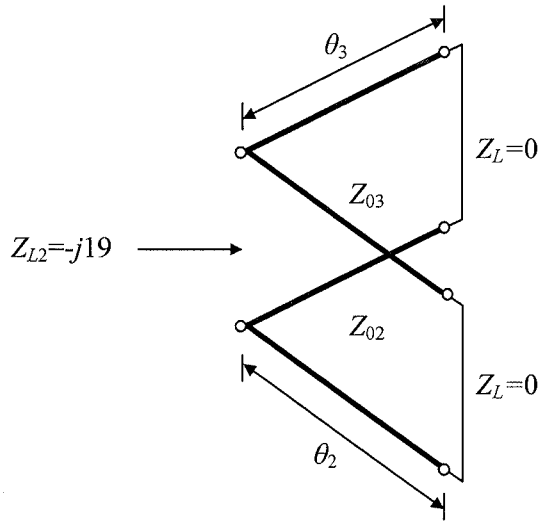


Figure 4.6: Transmission line circuit for Z_{L2}.

Further the length θ_3 is close to 90° (θ_3=87°) so that the dc voltage supply is isolated from the ac signal. The derivation of the formula for θ_3 is given in *Appendix 4C*.

$$\theta_3 = \frac{1}{2}\left(\pi + \tan^{-1}\left(\frac{1}{Z_{03}}\frac{Z_{L2}Z_{02}\tan 2\theta_2}{jZ_{02}\tan 2\theta_2 - Z_{L2}}\right)\right) \tag{4.1}$$

The frequency responses of the designed matching network for the fundamental frequency, second and third harmonic impedances are shown in Figure 4.7. For these three impedances it was found that the PAE was reduced by 1% from the optimum value obtained in Chapter 3.

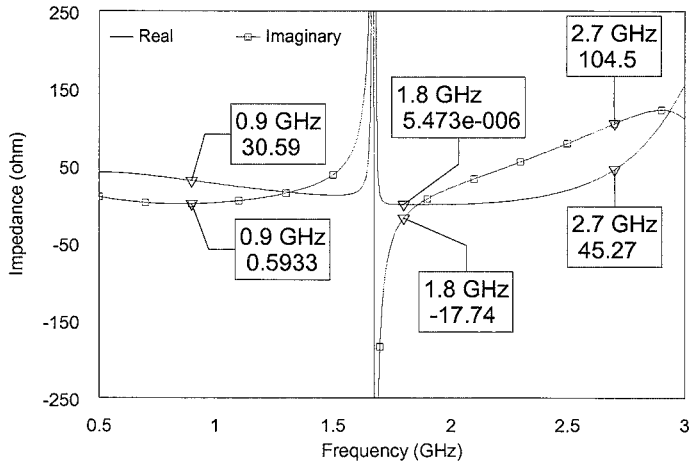
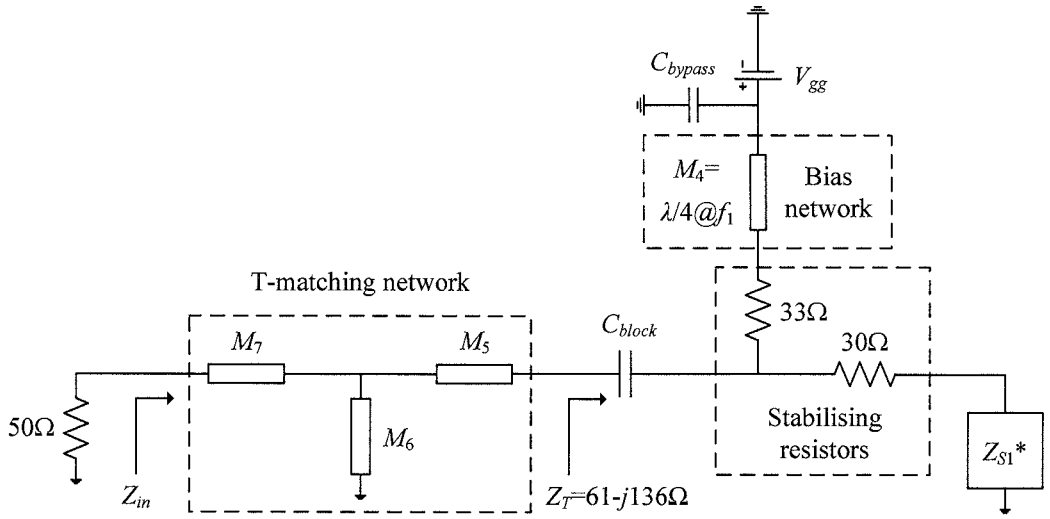


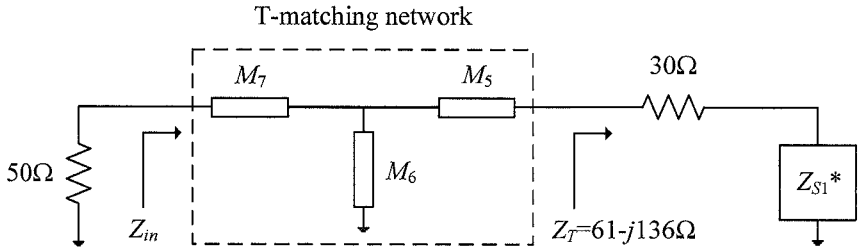
Figure 4.7: Simulated impedance response of the designed load matching network.

4.3.2 Source network for matching at the fundamental frequency

It was shown in Chapter 3 that the second and third harmonics source impedances have only a small effect on the PAE and therefore the source network was designed to produce a conjugate match at the fundamental frequency only. Figure 4.8(a) shows a three-element T-network consisting of a short circuit stub and two series transmission lines. As this network consists of three design elements it is possible to obtain a specified value of the Q-factor (and hence specify the bandwidth) and matching.



(a)



(b)

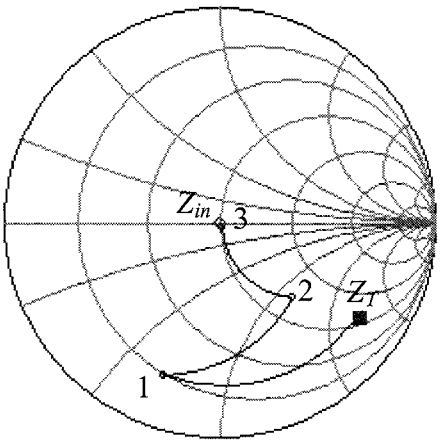
Figure 4.8: (a) Source matching network. (b) AC equivalent circuit.

In order to produce an open circuit at the junction of the stabilising resistors with the C_{block} the bias line, the value of M_4, is $\lambda/4@f_1$. The reactance of the C_{block} is very small, so that Z_T=61-j136 Ω.

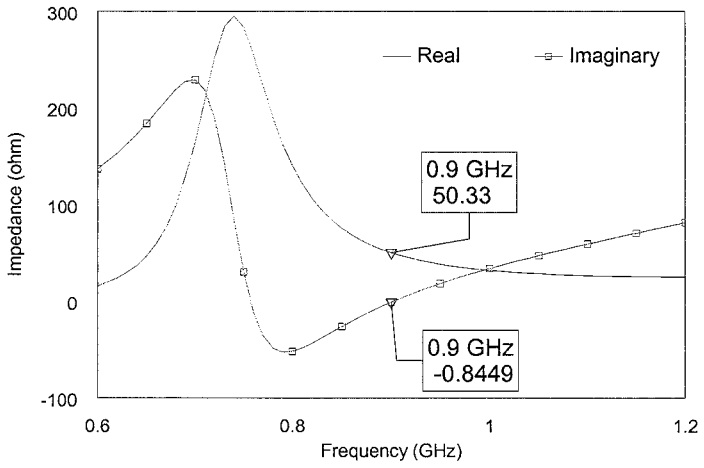
The return loss, S_{11} is obtained using equation (4.2).

$$S_{11} = 20\log\left(\frac{Z_{in}-50}{Z_{in}+50}\right) \tag{4.2}$$

Using the Smith chart approach the matching network was designed as shown in the sequences 1 to 3 in Figure 4.9(a), where Z_T is matched to the Z_{in} (=50 Ω). For the T-network the design characteristic impedances and lengths for three transmission lines are Z_{05}=55 Ω, Z_{06}=127 Ω, Z_{07}=127 Ω, θ_5=39°, θ_6=22°, θ_7=30°. The frequency response is shown in Figure 4.9(b), and the value, Z_{in}=50 Ω was obtained.



(a)



(b)

Figure 4.9: (a) Smith chart approach. (b) Simulated impedance response of the designed source matching network.

4.4 Practical Realisation and Results for the PA

The completed circuit design was implemented using a Duroid substrate with a thickness of 1.575 mm is shown in Figure 4.10. Using the ADS software tool the lengths and the widths of the microstrip lines were optimised. The parasitic effects of the dc block and RF bypass capacitors, stabilising resistors, and, discontinuities were taken into account. The dimensions of the microstrip lines and component values are listed in Table 4.1.

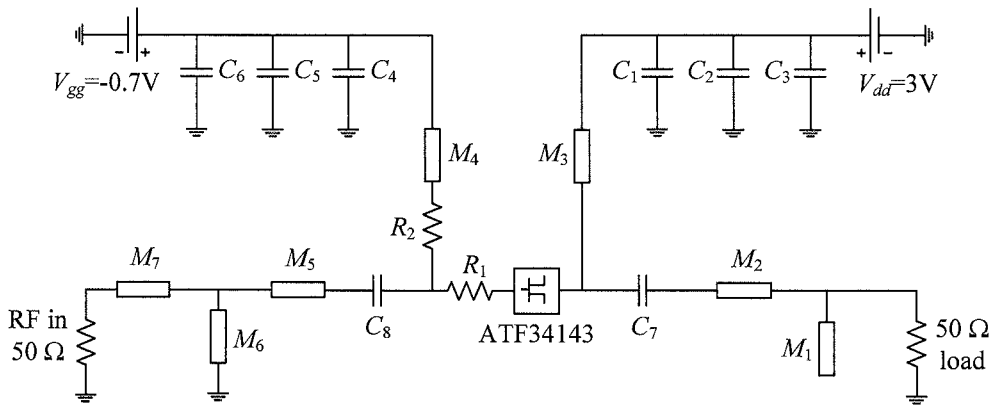


Figure 4.10: Circuit diagram of the PA.

C_1, C_4 (pF)	C_2, C_5 (pF)	C_3, C_6 (nF)	C_7 (pF)	C_8 (pF)	R_1 (Ω)	R_2 (Ω)
27	100	100	10	100	30	33
M_1	M_2	M_3	M_4	M_5	M_6	M_7
L=29 W=3.8	L=8 W=0.6	L=56 W=1.5	L=51 W=1.5	L=24.4 W=4	L=15.2 W=0.6	L=16.7 W=0.6

Table 4.1: Microstrip line dimensions (in mm) and component values.

To produce a broadband effective earth, three capacitors (C_1, C_2, C_3) were used at the drain terminal, and, three capacitors (C_4, C_5, C_6) were used at the gate terminal.

To ensure stability over the required frequency range two resistors R_1 and R_2 were used at the gate terminal (see Figure 4.10). From Figure 4.11 it can be seen that the active device is stable (μ>1) over the whole of the required frequency range.

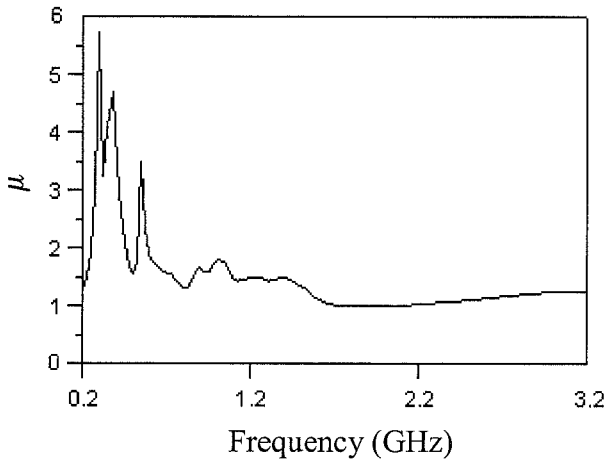


Figure 4.11: Simulated stability response.

The impedances Z_{L1}, Z_{L2}, Z_{L3} obtained in Chapter 3 from the load/source-pull method together with those obtained from the above network are shown in Figure 4.12. The numerical values are given in Table 4.2. As can be seen there is a close agreement between the two sets of impedances.

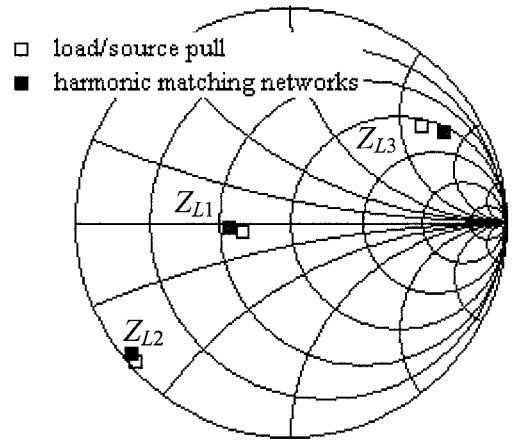


Figure 4.12: Simulated load impedances at P_{in}=8 dBm.

Harmonic	Load impedance, $Z_L(\Omega)$ obtained from load-pull	Load impedance, $Z_L(\Omega)$ obtained using the matching network
1	31.8-j2.7	28-j1.5
2	1-j19	1.4-j18
3	60+j125	61.9+j158

Table 4.2: Simulated load impedances at P_{in}=8 dBm.

Figure 4.13 shows that a good match has been obtained at the source terminal.

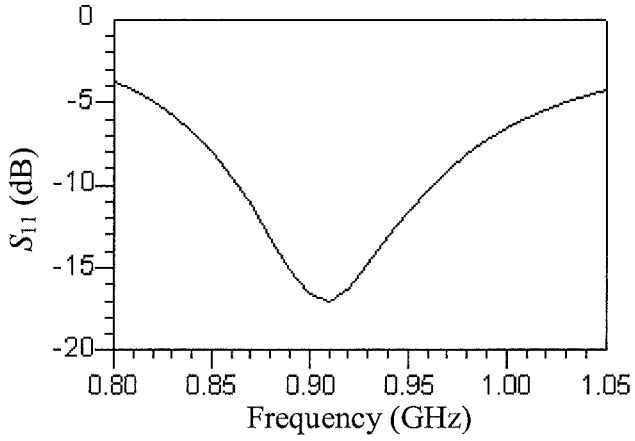


Figure 4.13: Simulated S_{11} at P_{in}=8 dBm (1.4-dB compression).

The return loss, S_{11}, is less than or equal to -10 dB over a frequency range 0.86-0.96 GHz, and, at the design frequency 0.9 GHz, S_{11} is -17 dB.

Figure 4.14 shows a comparison between the theoretical third harmonic-peaking (3^{rd} HP) [26] drain voltage/current waveforms and the simulated drain voltage/current waveforms.

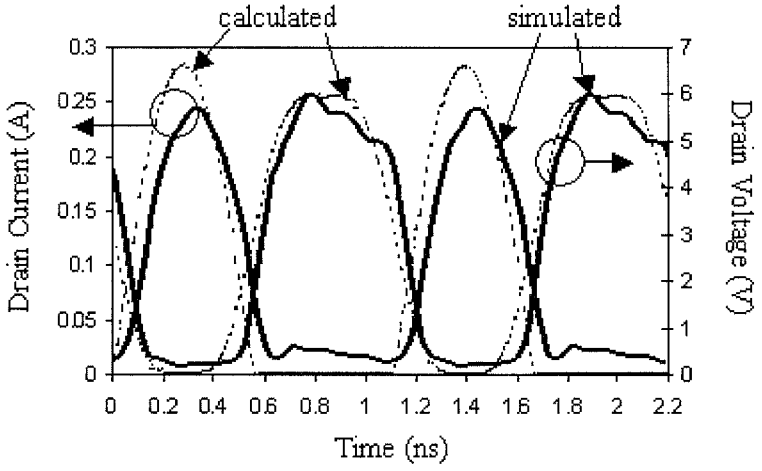


Figure 4.14: Calculated and simulated V_{ds} and I_{ds} waveforms at P_{in}=8 dBm.

Both sets of waveforms are in close agreement and show a minimum overlap between the almost square voltage and half-sinusoidal current waveforms. Consequently the power dissipated in the active device has been minimised and the efficiency has been maximised. However the simulated current waveform does exhibit a lower peak value than the calculated waveform. The reason for this is that the active device does not reach full pinch-off and the knee voltage is not zero so that the drain current is also not zero causing some power to be dissipated in the active device. Hence, the drain efficiency has been reduced from a theoretical value of 88.4% [26] to 74%.

Figure 4.15 shows that the output power P_{out} at the second harmonic (-17 dBm) and the third harmonic (-4.5 dBm) are much lower compared with the P_{out} at the fundamental frequency (22.3 dBm).

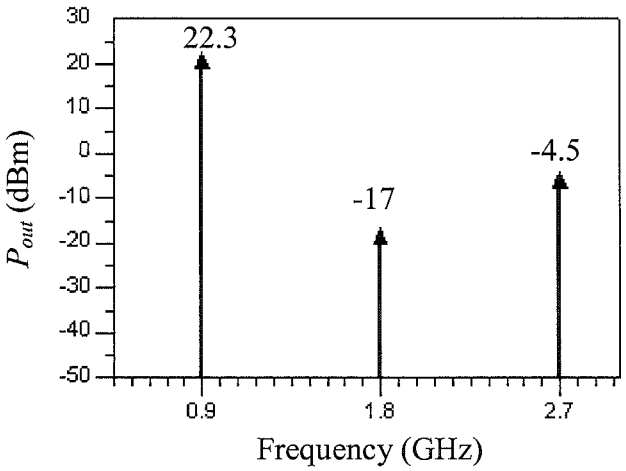


Figure 4.15: Simulated P_{out} spectrum at P_{in}=8 dBm.

The photograph of the designed PA is shown in Figure 4.16.

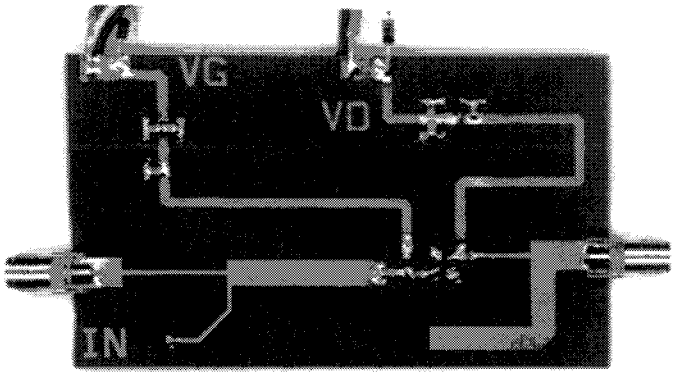


Figure 4.16: Photograph of the fabricated class-F PA.

Three via holes were added at the active device source to provide low inductance grounding. Zener diodes at the drain and gate bias networks were used to provide a protection against transients, reverse biasing and excessive voltages at the gate and drain terminals of the active device [83].

The measured and simulated results for PAE, P_{out} and G_p are shown in Figures 4.17 and 4.18 and are in very good agreement. The measured peak PAE was 71.4%, P_{out} was 22 dBm, and, a G_p of 14 dB G_p was obtained for an input power P_{in} of 8 dBm. The measured PAE is above 60% over a frequency range of 0.85-0.97 GHz.

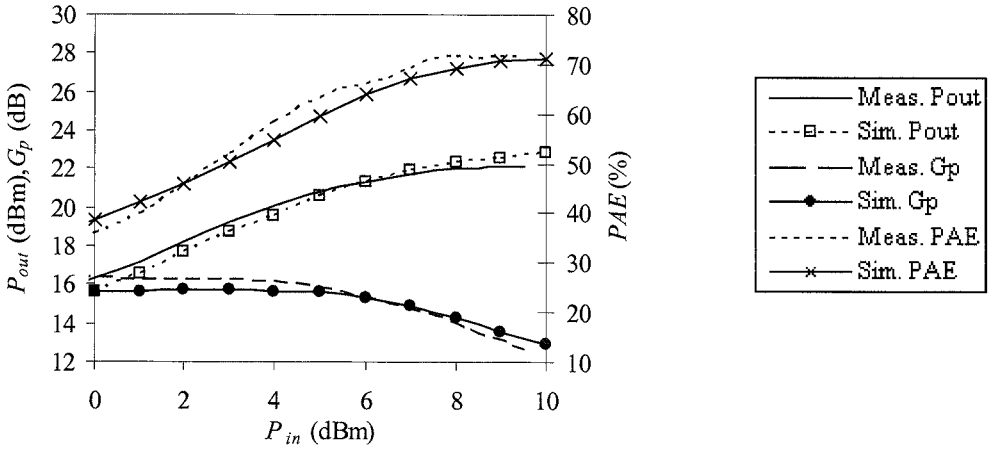


Figure 4.17: Measured and simulated PAE, G_p and P_{out} as a function of P_{in} at 0.9 GHz.

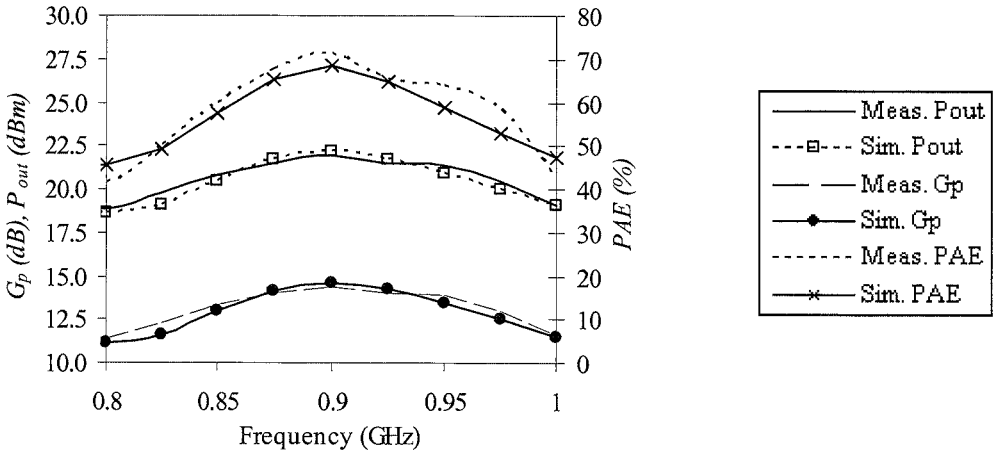


Figure 4.18: Measured and simulated PAE, G_p and P_{out} as a function of frequency at P_{in}=7.5 dBm.

4.5 Summary

To achieve the optimum load impedances from the load/source-pull method, a new proposed load harmonic matching network has been presented. A class-F PA with the source matching network and the new proposed load harmonic matching network, operating at 0.9 GHz, was designed and fabricated. No harmonic matching at the source terminal was needed since the nonlinearity of the gate capacitance is small.

The measured results obtained from this work are compared with the published results in Table 4.3 and in Figure 4.19 for class-F PAs using GaAs FET.

Reference	V_{dd} (V)	f_1 (GHz)	PAE (%)	P_{out} (dBm)
[70]	6	0.9	70	33
[71]	5.8	0.9	66	31.3
[72]	6	1.7	68	31.8
[73]	10	0.8	62	36.2
[74]	3	1.6	70	25
[75]	3	1.75	71	24.5
[78]	5	2	64.6	19.9
This work [68]	3	0.9	71.4	22

Table 4.3: Performances of GaAs FET class-F PAs with a load matching network.

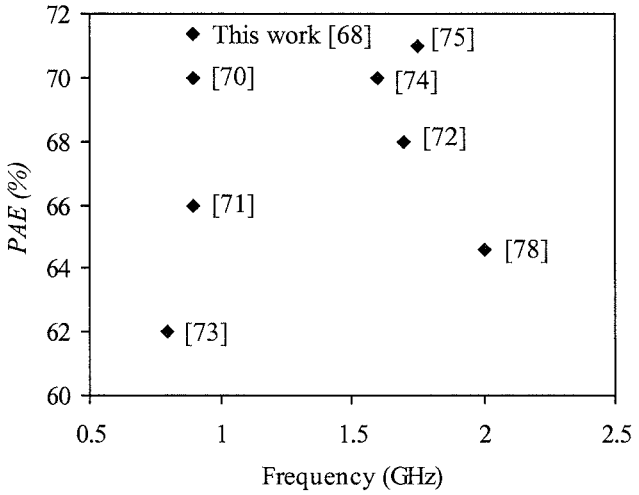


Figure 4.19: PAE of GaAs FET class-F PAs with a load matching network.

As can be seen the PAE obtained in this work is comparable with the results given in published papers. The output power is lower as only a medium power active device was available.

At the higher frequency of 2.45 GHz, the device capacitance is very nonlinear. The parasitic wiring inductances, and, package capacitances neglected at the lower frequency must be taken into account at the higher frequency. These problems have severe implications for harmonic terminations. In the following chapter the above difficulties are tackled at both the source and load terminals.

CHAPTER 5 DESIGN OF HIGH EFFICIENCY CLASS-F POWER AMPLIFIERS OPERATING AT 2.45 GHZ

5.1 Introduction

In this chapter two new proposed load and source harmonic matching networks are designed to investigate their effect on efficiency and harmonic suppression and matching capabilities. The first network is designed to meet the requirements for the optimum impedances of the load and source at the fundamental frequency and the second harmonic, while the second network is designed to meet the impedances at the fundamental frequency, the second and third harmonics. The synthesis method for the design of a network is normally used where the requirement is to produce either harmonic short or open circuit conditions. In the design of harmonic matching networks since it is necessary to obtain complex and finite reactive harmonic impedances, the synthesis method was not used. The matching networks are designed by the introduction of short circuit conditions at different sections of the circuit for each harmonic. This approach allows the matching sections at each frequency to be independently designed.

In Section 5.3 the load and source matching networks are designed to obtain the required impedances at the fundamental frequency and the second harmonic. The designed PA was realised using a Duroid substrate of thickness 0.79 mm. The simulated frequency responses for both source and load in the designed harmonic matching networks showed that the required impedances at the fundamental frequency and second harmonic were achieved. In Section 5.4 simulated stability factor, gate/drain waveforms, the return loss and the power spectrum at the first three harmonics are presented. Also, the simulated and measured results in terms of PAE, output power and power gain for the designed PA are presented. A good agreement between the simulated and practical results is obtained and a measured peak PAE of 74.5% was obtained.

In Section 5.5 details of the design of the new load and source harmonic matching for the fundamental frequency, and second and third harmonics are given. The frequency responses of the matching networks show that the required impedances were obtained. Similarly in Section 5.6 simulated results for stability, gate/drain waveforms, the return loss and the power spectrum are presented. The simulated and measured PAE, output power and power gain are compared and a measured peak PAE of 70.4% was obtained. This work has been published in [36].

5.2 Literature Survey of the Load and Source Matching Networks for Class-F PAs

The research reported in [66], [67], [84], [85] has shown that efficiency can be improved by using both the load and source harmonic matching networks rather than using only a load harmonic matching network.

Jeon [66] showed that when using only load harmonic matching network the low efficiency was caused by the nonlinearity of the gate capacitance distorting the waveform of the input signal. The nonlinear effect was then reduced by using a reversed biased diode at the gate of the active device, and, by simulation, an improved efficiency by 7% was obtained. In [67] the nonlinear effect of the gate capacitance was reduced by using a series L-C circuit and a lumped capacitor placed in parallel at the gate. A simulated efficiency of 81% was obtained at 5 GHz.

In [84] two $\lambda/4@f_1$ short circuit stubs, connected to the gate and drain terminals were used to produce short circuit conditions at the second harmonic. A measured PAE of 74% was obtained at 0.93 GHz. In [85] two-element low-pass networks were used at the source and load where the load network provided a short circuit at the second harmonic and an open circuit at third harmonic. The source network provided short circuits at the second and fourth harmonics. A measured PAE of 71% was obtained at 1.8 GHz.

In all the above designs it has been assumed that either open or short circuit conditions at the first few harmonic frequencies are required for maximum efficiency. However this is not the case for a practical active device [29], [37]. In [29] a T-network at the drain was used to obtain the required impedances at the fundamental frequency and second harmonic and a $\lambda/4@3f_1$ short circuit stub was used to obtain the required impedance at third harmonic. Also a source matching network was used to control the impedances at the fundamental frequency, and second and third harmonics. This design approach produced a PAE of 60% for a design frequency of 5 GHz. In [37] a $\lambda/4@f_1$ short circuit stub, and a microstrip line were used to control the load impedance at the second harmonic and an open circuit stub was used to control the load impedance at the third harmonic. At the source terminal, an open circuit stub and a $\lambda/4@f_1$ short circuit stub were used to control the second harmonic impedance. A PAE of 76% at 2 GHz was obtained.

5.3 Design of New Proposed Load and Source Matching Networks for the First Two Harmonics

In Chapter 3 optimum harmonic load and source impedances were obtained to achieve maximum efficiency. The load impedances at the fundamental frequency, second and third harmonics are Z_{L1}=36-j7 Ω, Z_{L2}=2-j61 Ω, Z_{L3}=1+j148 Ω, and, the source impedances are Z_{S1}=17+j28 Ω, Z_{S2}=5-j30 Ω, Z_{S3}=50+j220 Ω. In this section the load harmonic matching network was used in Chapter 4 for an operating frequency of 0.9 GHz, is employed to realise the optimum load and source impedances at the fundamental frequency and the second harmonic, for an operating frequency of 2.45 GHz.

The load matching network is shown in Figure 5.1. First the two-element L-C matching network (M_1, M_2) is used to transform the 50 Ω load to the optimum impedance Z_{L1} at the fundamental frequency.

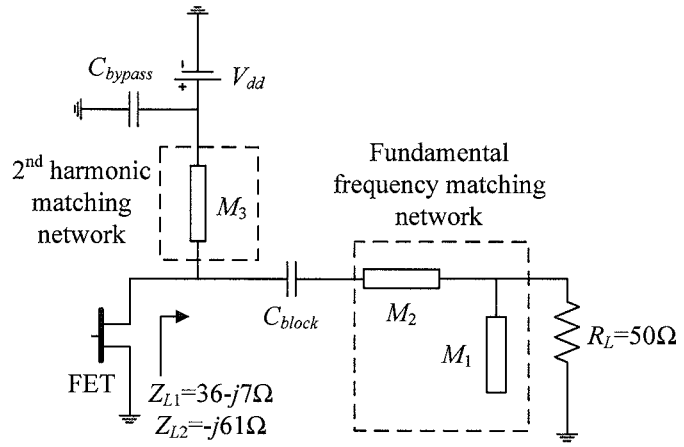
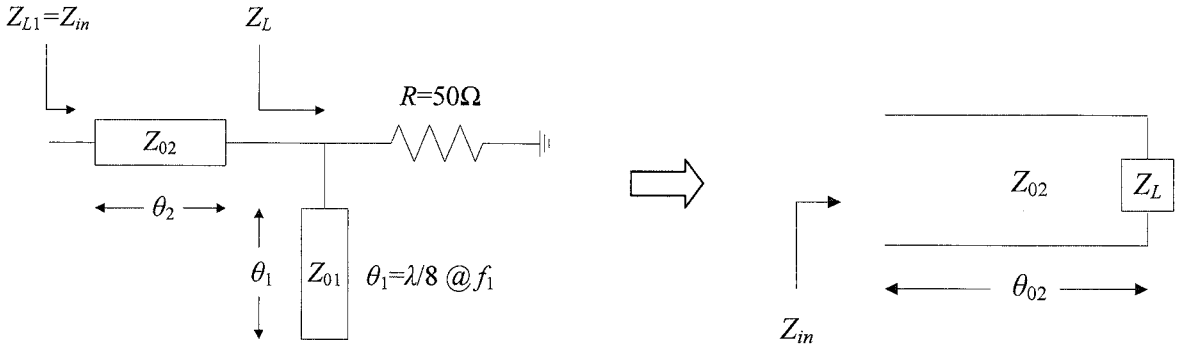


Figure 5.1: Load matching network for the first two harmonics.

In the matching circuit shown in Figure 5.2 there are four design parameters, Z_{01}, Z_{02}, θ_1 and θ_2 to be determined at the fundamental frequency.



(a) (b)

Figure 5.2: (a) AC equivalent circuit. (b) Transmission line circuit for Z_{L1}.

To ensure that the load impedance at the second harmonic, Z_{L2} is purely reactive the electrical length θ_1 is set to λ/8@f_1 in order to produce a short circuit condition at the junctions of the M_1, M_2 lines. The characteristic impedance Z_{01} was set to 100 Ω and the track width of the microstrip line was 0.6 mm. The load impedance Z_L (=R_L-jX_L) in Figure 5.2 is given by

$$Z_L = \left(\frac{jZ_{01}R}{jZ_{01} - R} \right) \tag{5.1}$$

where, R=50 Ω.

The input impedance Z_{in} is given by

$$Z_{in} = \frac{Z_{02}\left(R_L Z_{02}\left(1+\tan^2\theta_2\right)+j\left(Z_{02}\left(Z_{02}\tan\theta_2 + X_L\tan^2\theta_2 - X_L\right)-\left(R_L^{\,2}+X_L^{\,2}\right)\tan\theta_2\right)\right)}{\left(Z_{02}+X_L\tan\theta_2\right)^2+\left(R_L\tan\theta_2\right)^2} \tag{5.2}$$

With Z_{in}=Z_{L1}=36-j7 Ω equating the real and imaginary parts in equation (5.2) it can be shown that Z_{02}=67.5 Ω and θ_2=15.1°. The derivation of the formula for θ_2 and Z_{02} is given in *Appendix 5A*.

The frequency response of this circuit is shown in Figure 5.3 where, at 2.45 GHz, the optimum value of Z_{L1}=36-j7 Ω is obtained. However at the second harmonic the load impedance Z_{L2}=j39.3 Ω does not match the required value, -j61 Ω.

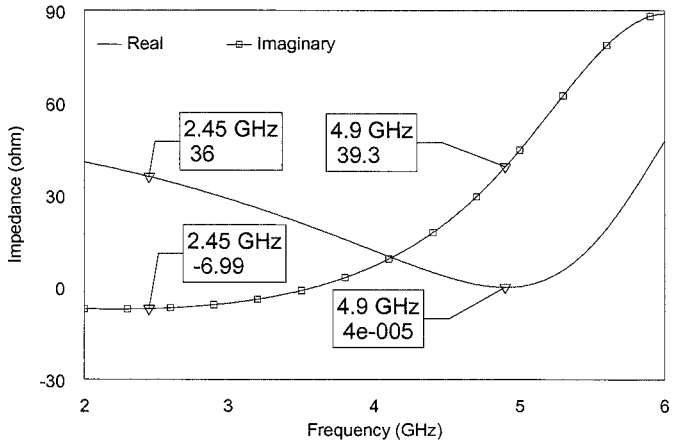
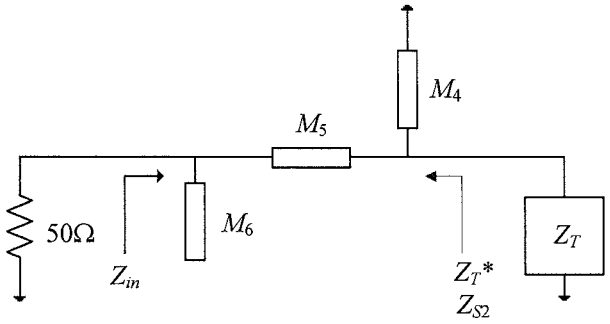


Figure 5.3: Simulated impedance response of the two-element L-C matching network.

In order to realise the impedance at the second harmonic the method discussed in Chapter 4 is used to obtain the electrical length of the line M_3, (θ_3=83.3°). The frequency response of the designed load harmonic matching network is shown in Figure 5.4 where Z_{L2}=-j60.7 Ω was obtained together with an insignificant change in Z_{L1} (=36.5-j5.5 Ω). However, the impedance obtained by this network for the third harmonic is different (Z_{L3} =64.6+j57.6 Ω) from the required optimum.



(b)

Figure 5.5: (a) Source matching network for the first two harmonics. (b) AC equivalent circuit.

The electrical lengths (θ_{04}=75.3°, θ_{05}=64° and θ_{06}=45°) and characteristic impedances (Z_{04}=100 Ω, Z_{05}=50.2 Ω, Z_{06}=45 Ω) of lines M_4, M_5 and M_6 were obtained as for the load network as discussed above.

As shown in Figure 5.6 the required optimum impedances at the fundamental frequency and second harmonic have been obtained. However, the impedance obtained by this network for the third harmonic is different (Z_{S3} =15.1+j30.2 Ω) from the required optimum.

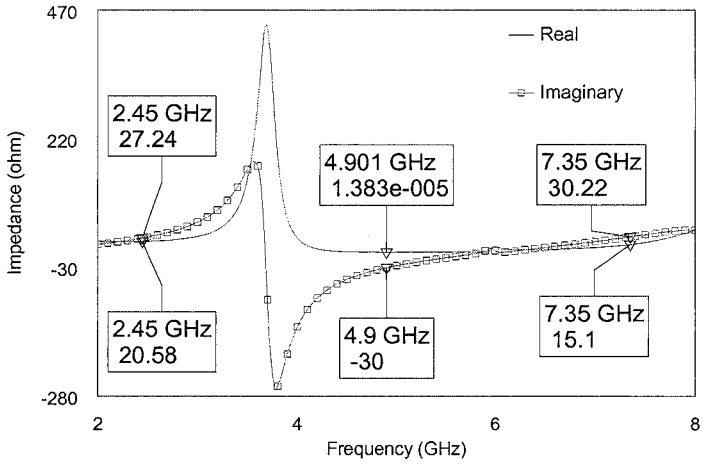


Figure 5.6: Simulated impedance response of the designed source matching network.

The simulated PAE for the complete circuit in transmission line form shows that a simulated PAE of about 74% was obtained, which is very close to the result obtained from the load/source-pull method. In the following section the practical realisation and results for the PA are presented, while, in Section 5.5 a new matching network is introduced to obtain optimum source and load impedances at all three harmonics.

5.4 Practical Realisation and Results for the PA

The designed source and load harmonic transmission lines matching networks were transformed into microstrip lines. The lengths and the widths of the microstrip lines were fine tuned using the ADS software tool in order to take into account the effects of dc block capacitors, RF bypass capacitors, stabilising resistors and discontinuities. The complete circuit of the PA is shown in Figure 5.7 and the dimensions of the microstrip lines and values of the circuit components are given in Table 5.1.

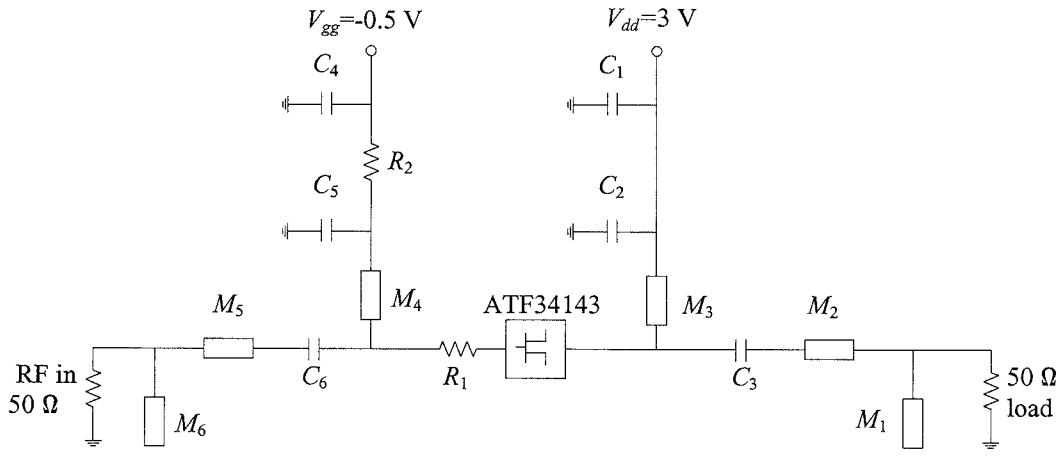


Figure 5.7: Circuit diagram of the PA.

C_1, C_4 (nF)	C_2 (pF)	C_3 (pF)	C_5 (pF)	C_6 (pF)	R_1 (Ω)	R_2 (Ω)
10	4.7	3	4.3	9.1	6.8	33

M_3	M_2	M_1	M_4	M_5	M_6
L=19.8 W=0.4	L=5.9 W=2.3	L=10.9 W=0.6	L=19 W=0.4	L=7 W=2.3	L=11 W=1

Table 5.1: Microstrip line dimensions (in mm) and component values.

The stability factor μ of the PA shown in Figure 5.8 is greater than unity so there is unconditional stability over the plotted frequency range.

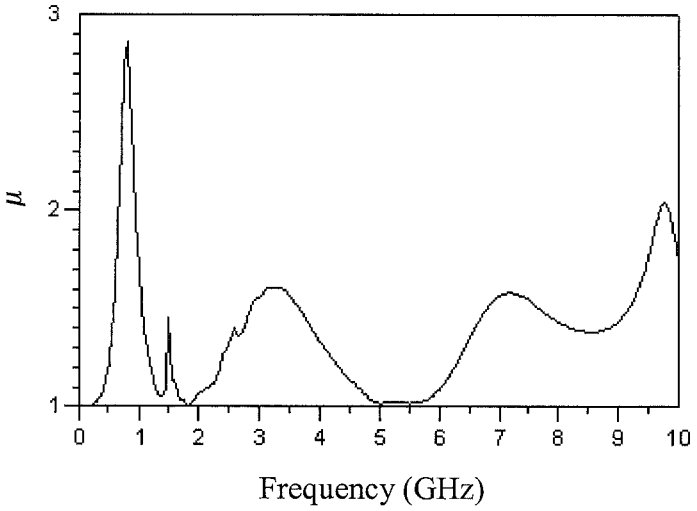


Figure 5.8: Simulated stability response.

The load and source harmonic impedances obtained from the load/source-pull method and those obtained by the designed matching networks are shown on the Smith chart in Figure 5.9 and also in Table 5.2. An excellent agreement between the obtained and required impedances at the fundamental frequency and second harmonic has been obtained.

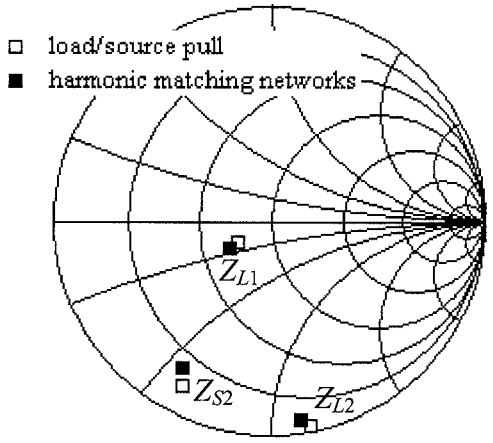


Figure 5.9: Simulated load and source impedances at P_{in}=13 dBm.

	Load/Source Impedance, $Z_L(\Omega)$, $Z_S(\Omega)$ Obtained from Load/Source-Pull	Load/Source Impedance, $Z_L(\Omega)$, $Z_S(\Omega)$ Obtained using Matching Networks
Z_{L1}	36-*j*7	33-*j*9
Z_{L2}	2-*j*61	4-*j*58.5
Z_{S2}	5-*j*30	7.5-*j*28

Table 5.2: Simulated load and source impedances at P_{in}=13 dBm.

The simulated frequency response of S_{11} is shown in Figure 5.10 for an input power P_{in} of 9.5 dBm. S_{11} of -14.7 dB is obtained at 2.45 GHz.

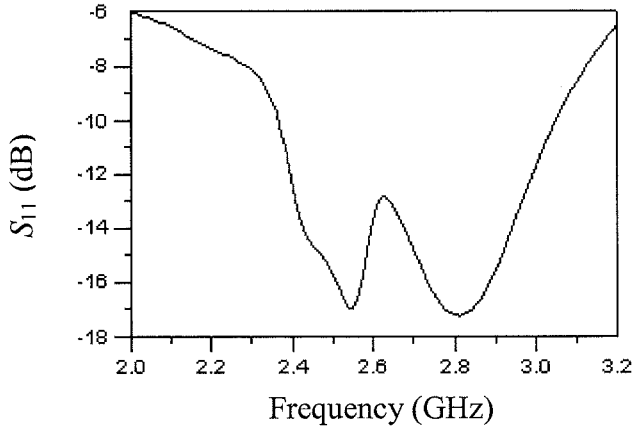


Figure 5.10: Simulated S_{11} at P_{in}=9.5 dBm (2.1-dB compression).

A simulated gate voltage waveform is shown in Figure 5.11 where a nearly equal on-off duty cycle is obtained.

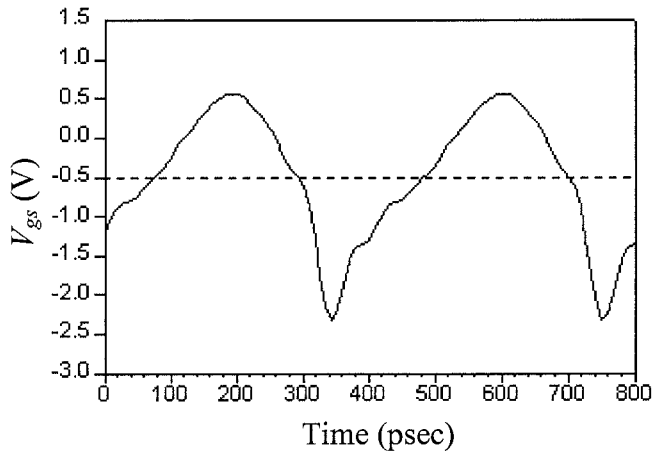


Figure 5.11: Simulated V_{gs} waveform at 2.45 GHz with P_{in}=9.5 dBm.

This waveform as suggested in [66] and [67], indicates that the strong nonlinearity of the gate capacitance (see Chapter 3) has been compensated for by using the designed source harmonic matching network.

Figure 5.12 shows optimum waveforms for the drain voltage and current. The overlapping area between the current and voltage waveforms is small so that the power dissipated in the active device is correspondingly small, hence the PAE is increased.

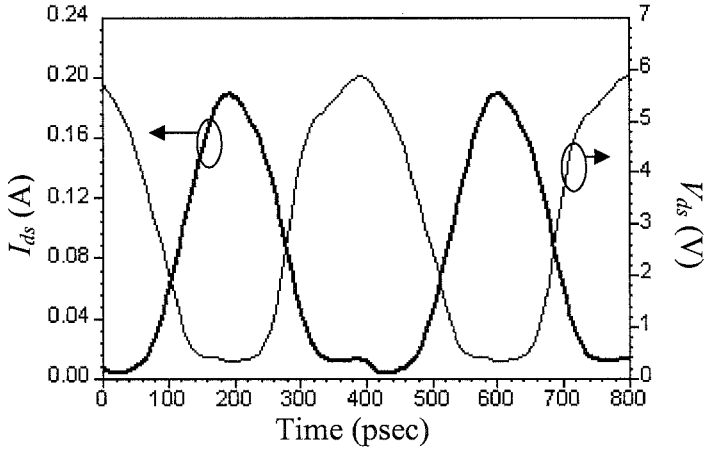


Figure 5.12: Simulated V_{ds} and I_{ds} waveforms at 2.45 GHz with P_{in}=9.5 dBm.

Figure 5.13 shows the simulated output power spectrum at the first three harmonics where the power at the fundamental frequency is 21.35 dBm.

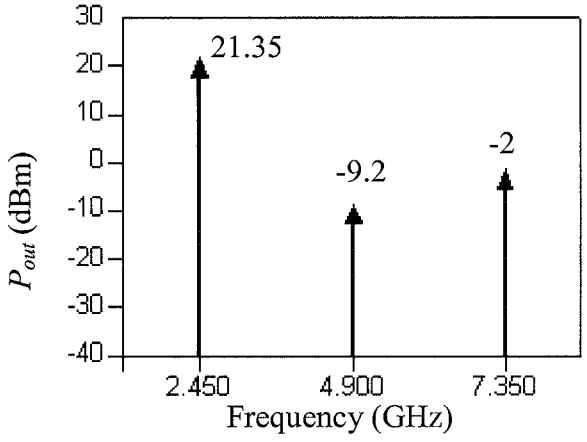


Figure 5.13: Simulated P_{out} spectrum at P_{in}=9.5 dBm.

The power at the second harmonic and the third harmonic is -9.2 dBm and -2 dBm respectively which are well below the output power at the fundamental frequency. As discussed in the next section the output power of the third harmonic is reduced. This is the result of the load harmonic network being designed to obtain the optimum impedances at the fundamental frequency, second and third harmonics.

The fabricated PA is shown in Figure 5.14.

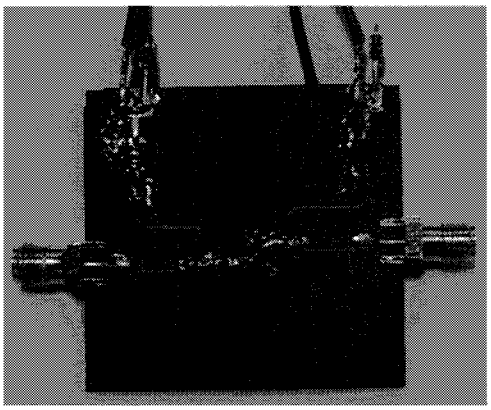


Figure 5.14: Photograph of the fabricated PA.

The simulated and measured PAE as a function of P_{in} are shown in Figure 5.15. A maximum PAE of 74.5% was achieved at 2.45 GHz with P_{in}=12 dBm.

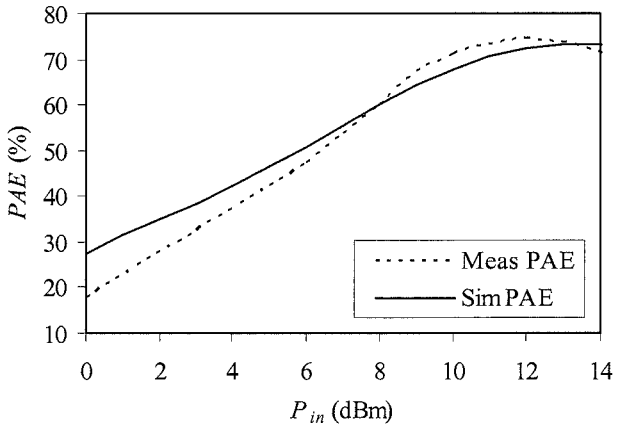


Figure 5.15: Simulated and measured PAE as a function of P_{in} at 2.45 GHz.

The simulated and measured P_{out} and G_p as a function of P_{in} is shown in Figure 5.16, where a measured P_{out} of 21.21 dBm and G_p of 9.21 dB was obtained. Good agreement between the simulated and practical results over the range of P_{in} has been obtained.

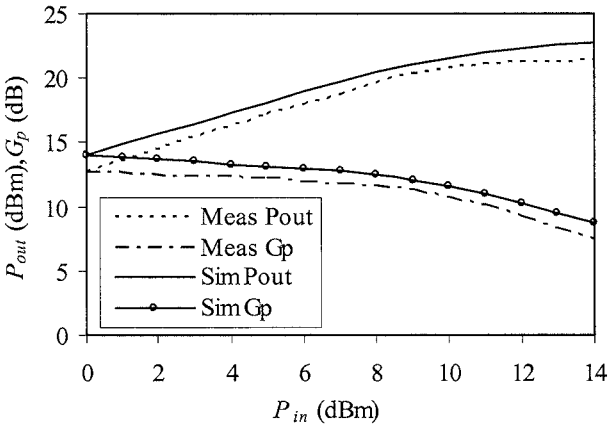


Figure 5.16: Simulated and measured G_p and P_{out} as a function of P_{in} at 2.45 GHz.

The simulated and measured P_{out} and G_p as a function of frequency are shown in Figure 5.17.

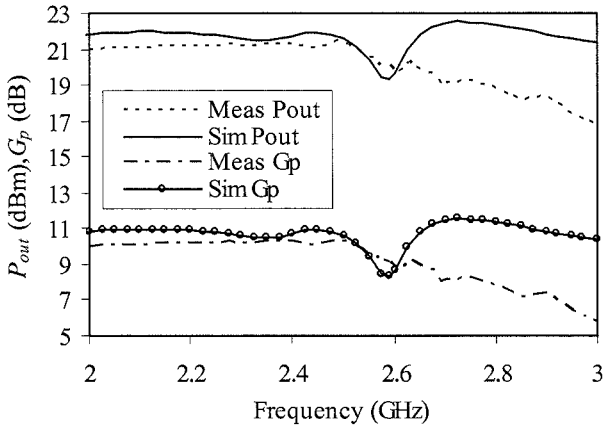


Figure 5.17: Simulated and measured G_p and P_{out} as a function of frequency at P_{in}=11 dBm.

The simulated and measured PAE as a function of frequency are shown in Figure 5.18. There is also a good agreement between the simulated and measured efficiency over the frequency range 2-3 GHz.

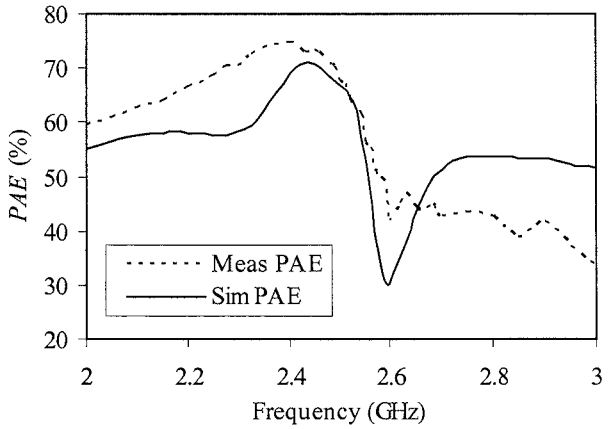


Figure 5.18: Simulated and measured PAE as a function of frequency at P_{in}=11 dBm.

For the practical PA, in the frequency range 2.05-2.54 GHz, a value of at least 60% for the PAE with a minimum P_{out} of 20.75 dBm is obtained. In Figure 5.18 the efficiency drops sharply at 2.6 GHz. This is due to the change of the reactance from capacitive to inductive in the frequency response of the designed load matching network (see Figure 5.4).

5.5 Design of New Proposed Load and Source Matching Networks for the First Three Harmonics

In Section 5.3 only the load and source matching networks for the fundamental frequency and second harmonic were designed to meet the requirements for maximum efficiency. In order to investigate the importance of meeting the requirement for the third harmonic a new harmonic matching network is introduced in this section. In the following section the practical results for the designed PA are presented.

The proposed load harmonic matching network is shown in Figure 5.19 where four transmission lines M_1, M_2, M_3 and M_4 are used for matching the second and third harmonic impedances. As discussed below the eight unknown parameters (θ_1, θ_2, θ_3, θ_4, Z_{01}, Z_{02}, Z_{03}, Z_{04}) are obtaining by isolated short circuit conditions at the second and third harmonics.

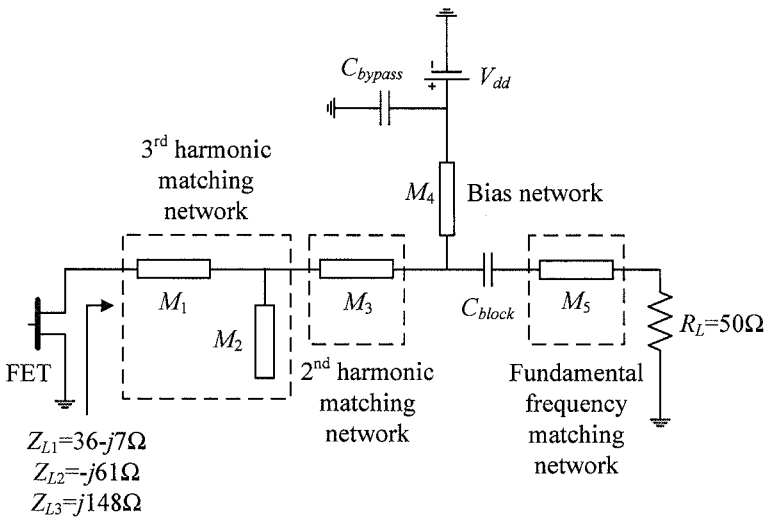


Figure 5.19: Load matching network for the first three harmonics.

The required optimum load impedances at the fundamental frequency, second and third harmonics are, Z_{L1}=36-j7 Ω, Z_{L2}=2-j61 Ω and Z_{L3}=1+j148 Ω. The length of M_2 is assumed to be $\lambda/4@3f_1$ so that an effective short circuit is produced at the junction of the lines M_1, M_2 and M_3 at the third harmonic. Hence the rest of the circuit after this junction does not affect the third harmonic impedance. The characteristic impedance of M_2 is not critical and was therefore assumed to be 100 Ω. The characteristic impedance of line M_1, Z_{01} was also assumed to be 100 Ω and its length of θ_1 (=18.7°) was determined from equation (5.3). The derivation of the formula for θ_1 is given in *Appendix 5B*.

$$\theta_1 = \frac{1}{3}\tan^{-1}\left(\frac{-jZ_{L3}}{Z_{01}}\right) \tag{5.3}$$

To isolate the dc voltage source from the ac signals the length of line M_4 was assumed to be $\lambda/4@f_1$ with a high characteristic impedance of Z_{04}=100 Ω. At the second harmonic this length also produces a short circuit condition at the junction of M_3, M_4, and the C_{block}. The equivalent circuit at the second harmonic used to obtain the optimum load impedance Z_{L2}=-j61 Ω is shown in Figure 5.20. Assuming that Z_{03} is equal to 50 Ω, the electrical length θ_3 is equal to 28.1° which is obtained from equation (5.4) which is derived in *Appendix 5C*.

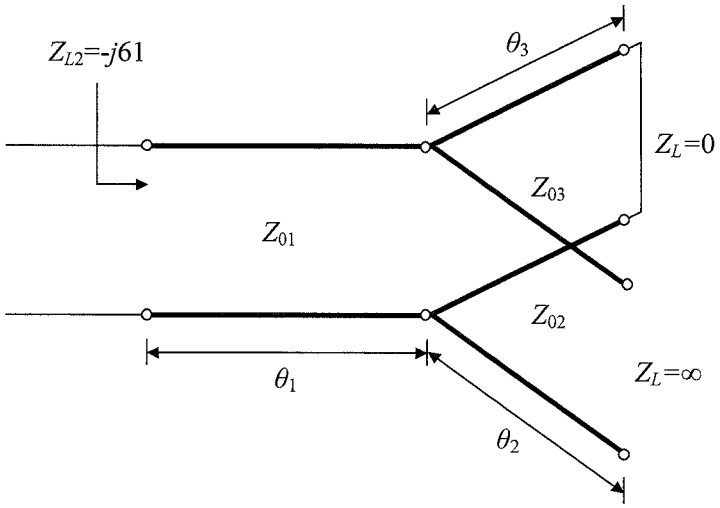
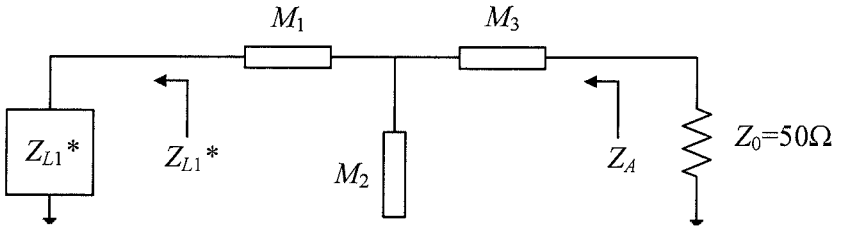


Figure 5.20: Transmission line circuit for Z_{L2}.

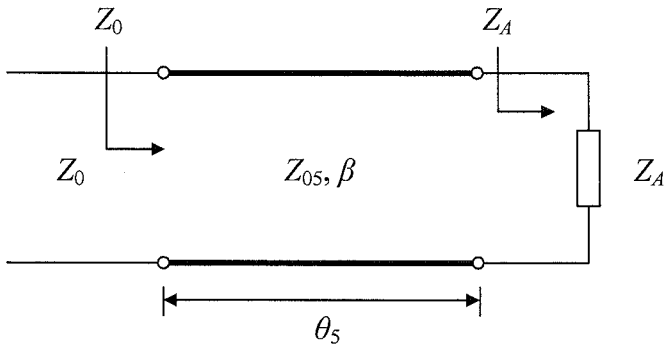
$$\theta_3 = \frac{1}{2}\tan^{-1}\left(\frac{Z_{01}Z_{02}}{Z_{03}}\frac{\tan\left(\tan^{-1}\left(\frac{-jZ_{L2}}{Z_{01}}\right)-2\theta_1\right)}{Z_{02}+1.732Z_{01}\left(\tan\left(\tan^{-1}\left(\frac{-jZ_{L2}}{Z_{01}}\right)-2\theta_1\right)\right)}\right) \tag{5.4}$$

Further, as an effective open circuit is produced at the junctions of M_3, M_4, and C_{block} at the fundamental frequency, the rest of the circuit is isolated and the transmission line M_5 can be used to obtain matching at the fundamental frequency. In order to produce matching the electrical length θ_5 and the characteristic impedance Z_{05} of the line M_5 must be obtained.

In the equivalent circuit of the matching network shown in Figure 5.21(a) all the parameters are known so that the impedance Z_A at the fundamental frequency was found to be 85.3-j1.3 Ω. In Figure 5.21(b) M_5 acts as a transformer to match Z_A to 50 Ω.



(a)



(b)

Figure 5.21: (a) AC equivalent circuit. (b) Simple matching network.

The characteristic impedance Z_{05} (=65.3 Ω) of the microstrip line is given by [86]

$$Z_{05} = \sqrt{Z_0 \frac{\left(Z_0 R - R^2 - X^2\right)}{Z_0 - R}} \tag{5.5}$$

where, Z_0=50 Ω while the electrical length θ_5 (=88.4°) is given by [87]

$$\theta_5 = \tan^{-1}\left(jZ_{05} \frac{Z_A - Z_0}{Z_{05}^{\ 2} - Z_A Z_0} \right) \tag{5.6}$$

The frequency response of the designed matching network for the first three harmonic impedances Z_{L1}=36-j6.8 Ω, Z_{L2}=-j60.3 Ω, Z_{L3}=j148.8 Ω, is shown in Figure 5.22.

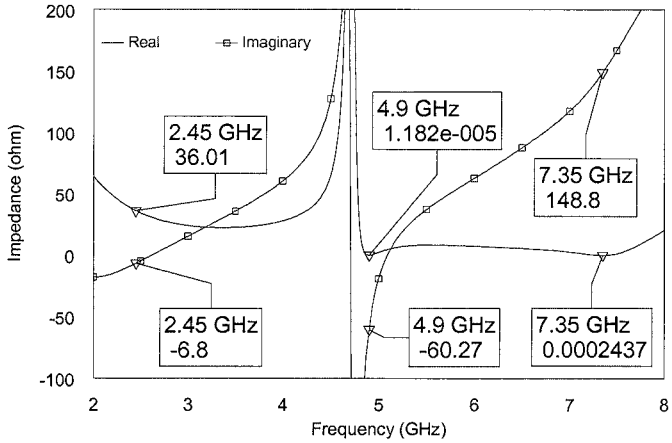
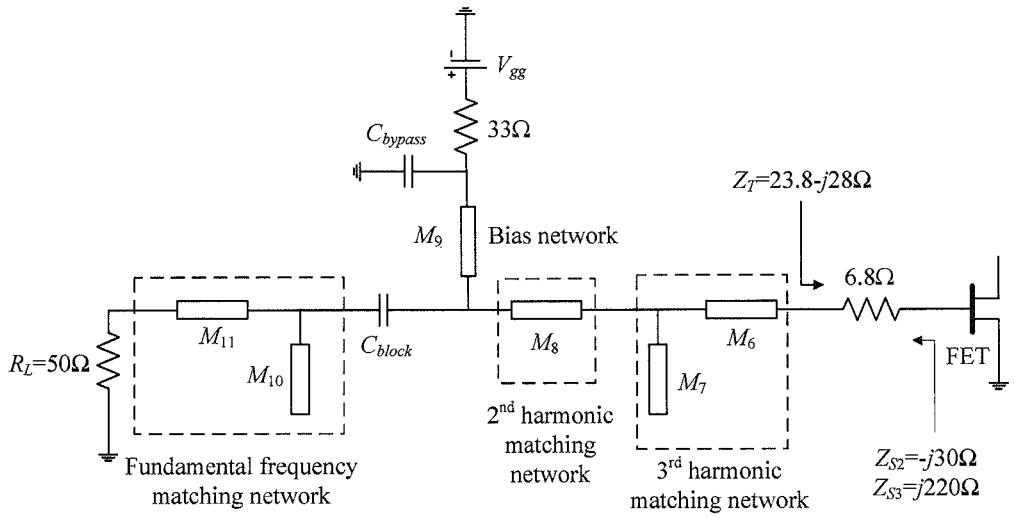
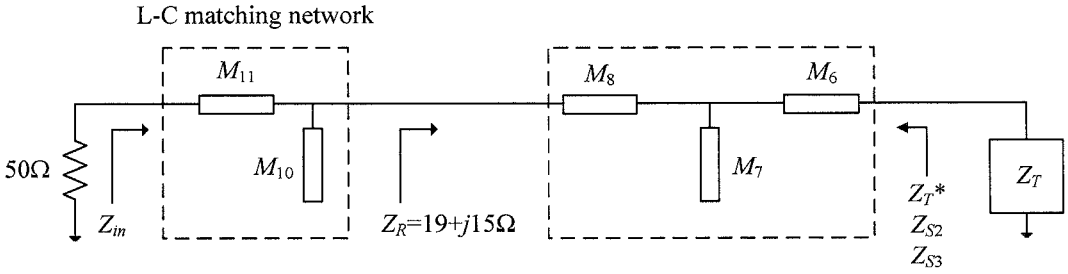


Figure 5.22: Simulated impedance response of the designed load matching network.

A source harmonic matching network similar to the one used for the load is shown in Figure 5.23(a) and its ac equivalent circuit is shown in Figure 5.23(b).



(a)



(b)

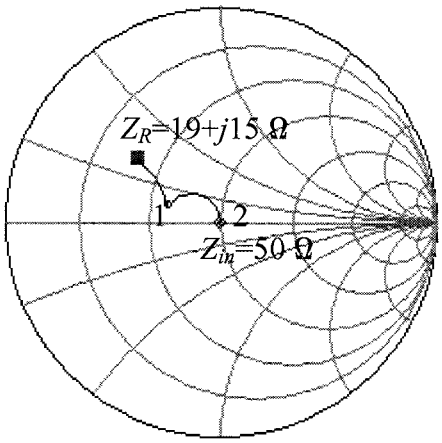
Figure 5.23: (a) Source matching network. (b) AC equivalent circuit.

The main difference between the load and source matching networks is that for matching at the fundamental frequency it was not possible to use a length of transmission line (M_5 in Figure 5.19) as the width of the required microstrip line is too great. Consequently a two-element L-C matching network consisting of lines M_{10}, M_{11} was used.

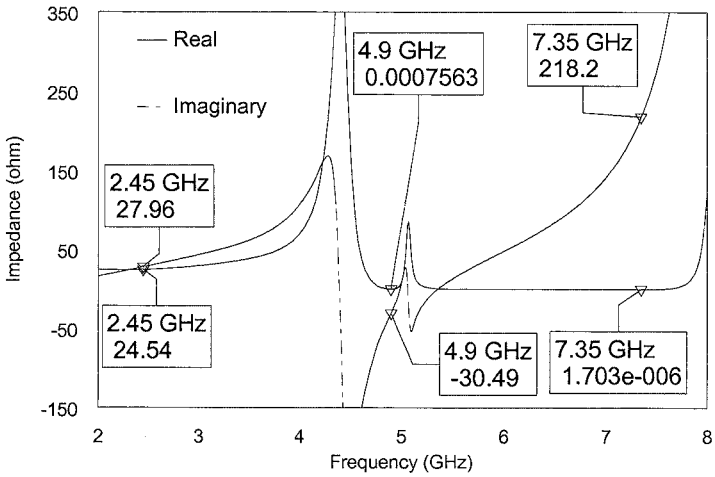
The required impedance at the third harmonic was controlled by lines M_6, M_7 and the required impedance at the second harmonic was controlled by lines M_8, M_9. Electrical lengths (θ_{06}=24.5°, θ_{07}=30°, θ_{08}=12° and θ_{09}=90°) of lines M_6, M_7, M_8 and M_9 were obtained as for the load network. The characteristic impedances of these lines were Z_{06}=65 Ω, Z_{07}=65 Ω, Z_{08}=100 Ω, Z_{09}=100 Ω.

At the fundamental frequency the conjugate matching was then achieved by using a two-element L-C matching network (M_{10} and M_{11}), which transformed the impedance Z_R to

approach 50 Ω following the sequence Z_R, 1, 2 as shown on the Smith chart (see Figure 5.24(a). The values of Z_{10}=42 Ω, Z_{11}=38 Ω, θ_{10}=38.9°, θ_{11}=69.8° were obtained. The frequency response of the designed network is shown in Figures 5.24(b) where the required impedances for the three frequencies have been obtained.



(a)



(b)

Figure 5.24: (a) Smith chart approach. (b) Simulated impedance response of the designed source matching network.

The simulated PAE for the complete circuit in transmission line form shows that a simulated PAE of 75.3% was obtained, which is slightly higher than that of the PA with matching for the first two harmonics (see Section 5.3). In the following section the practical realisation and results for the PA are presented.

5.6 Practical Realisation and Results for the PA

The complete circuit of the PA is shown in Figure 5.25 and the optimised dimensions of the microstrip lines and components values are given in Table 5.3.

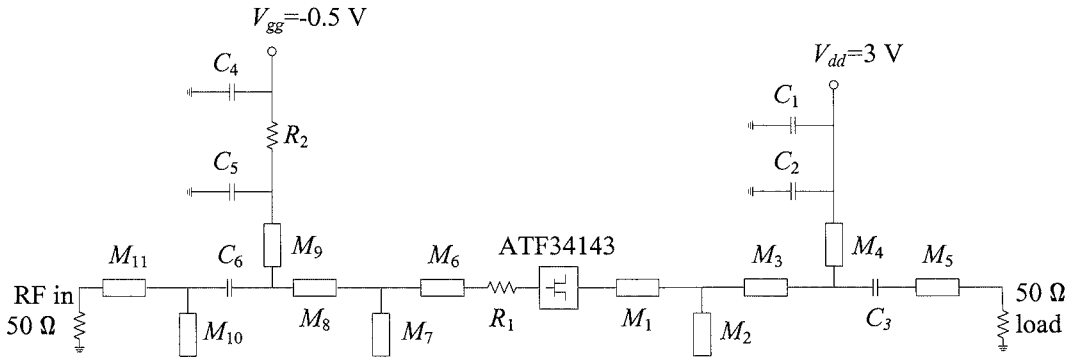


Figure 5.25: Circuit diagram of the PA.

C_1, C_4 (nF)		C_2 (pF)		C_3 (pF)		C_5 (pF)		C_6 (pF)		R_1 (Ω)		R_2 (Ω)	
10		4.7		100		4.3		9.1		6.8		33	
M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	M_9	M_{10}	M_{11}			
L=4	L=7.5	L=5.7	L=21.3	L=18	L=2.2	L=7.5	L=1.9	L=22	L=9	L=6			
W=0.6	W=0.6	W=3	W=1	W=1.6	W=1.5	W=1.5	W=0.6	W=0.6	W=3	W=3			

Table 5.3: Microstrip line dimensions (in mm) and component values.

The frequency response of the stability factor μ in Figure 5.26 shows that the designed PA is unconditionally stable over the frequency range 0.3-10 GHz.

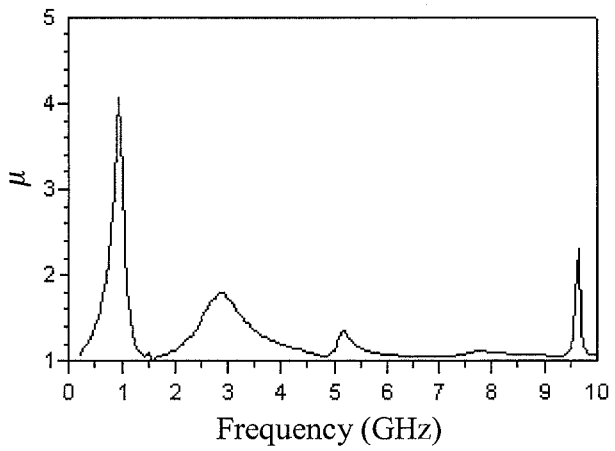


Figure 5.26: Simulated stability response.

The load and source optimum impedances, and, those obtained by the designed matching networks for the fundamental frequency, the second and third harmonics are compared on the Smith chart in Figure 5.27 and in Table 5.4. A good agreement for all the impedances has been obtained.

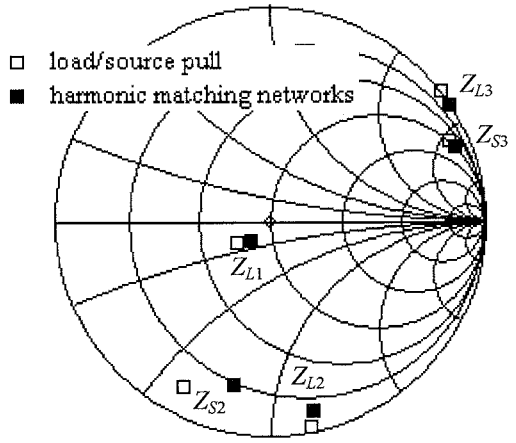


Figure 5.27: Simulated load and source impedances at P_{in}=13 dBm.

	Load/Source Impedance, $Z_L(\Omega)$, $Z_S(\Omega)$ Obtained from Load/Source-Pull	Load/Source Impedance, $Z_L(\Omega)$, $Z_S(\Omega)$ Obtained using Matching Networks
Z_{L1}	36-j7	41-j7.7
Z_{L2}	2-j61	7-j62
Z_{L3}	1+j148	2+j168
Z_{S2}	5-j30	10.5-j39
Z_{S3}	50+j220	53+j243

Table 5.4: Simulated load and source impedances at P_{in}=13 dBm.

The frequency response of S_{11} is shown in Figure 5.28 where over -20 dB has been obtained over a frequency range 2.4-2.65 GHz.

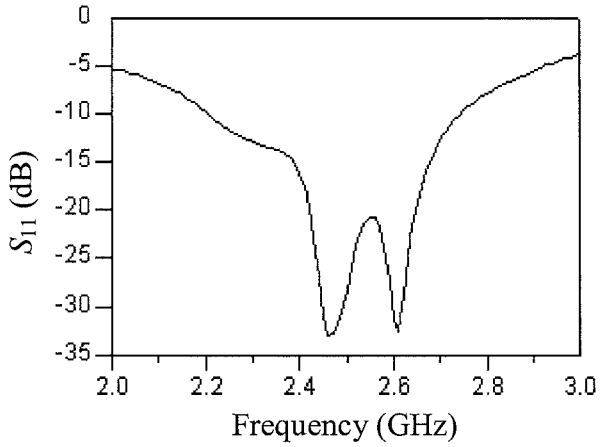


Figure 5.28: Simulated S_{11} at P_{in}=9 dBm (2.2-dB compression).

The simulated gate voltage and the drain current/voltage waveforms are shown in Figures 5.29 and 5.30.

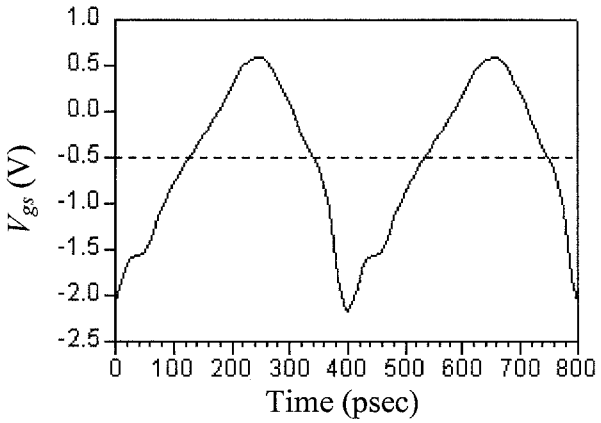


Figure 5.29: Simulated V_{gs} waveform at 2.45 GHz with P_{in}=9 dBm.

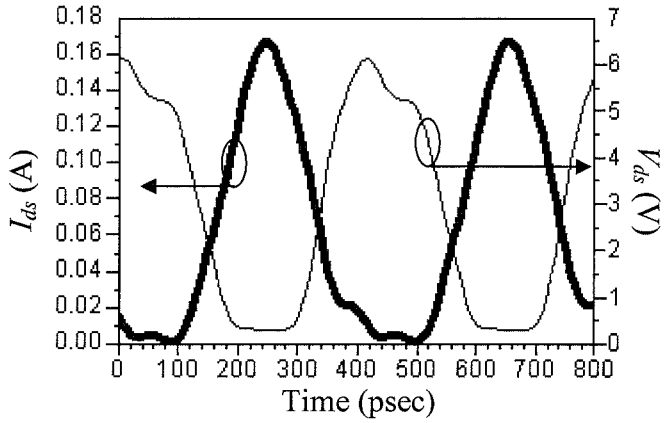


Figure 5.30: Simulated V_{ds} and I_{ds} waveforms at 2.45 GHz with P_{in}=9 dBm.

A nearly symmetric gate voltage waveform (see Figure 5.29) is obtained. Also as can be seen in Figure 5.30 the overlapping area between the drain current and voltage waveforms is small and therefore a high efficiency is obtained for the PA circuit.

As shown in Figure 5.31 the output power at the second and third harmonics are 28.2 dB and 42.9 dB which are lower than the output power at the fundamental frequency.

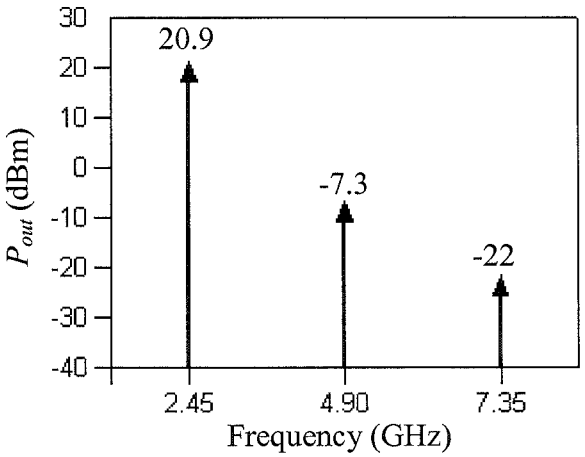


Figure 5.31: Simulated P_{out} spectrum at P_{in}=9 dBm.

A photograph of the fabricated PA is shown in Figure 5.32.

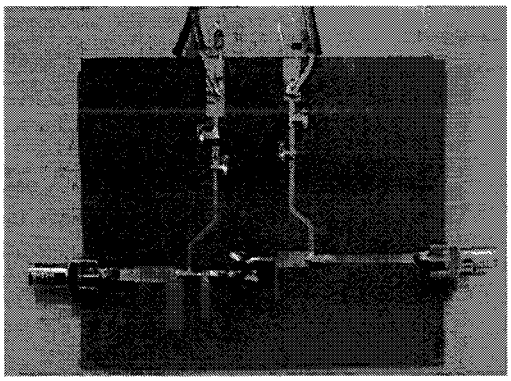


Figure 5.32: Photograph of the fabricated PA.

The simulated and measured PAE as a function of P_{in} are shown in Figure 5.33. The simulated and measured P_{out} and G_p responses are shown in Figure 5.34.

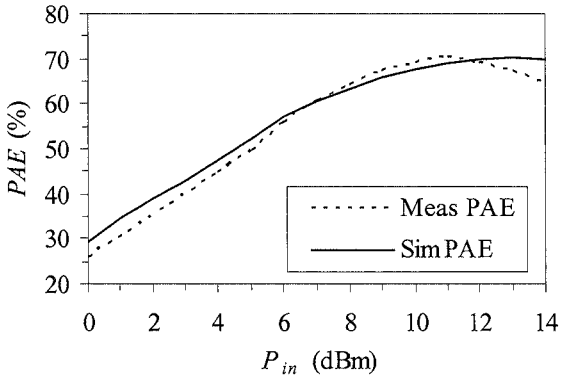


Figure 5.33: Simulated and measured PAE as a function of P_{in} at 2.45 GHz.

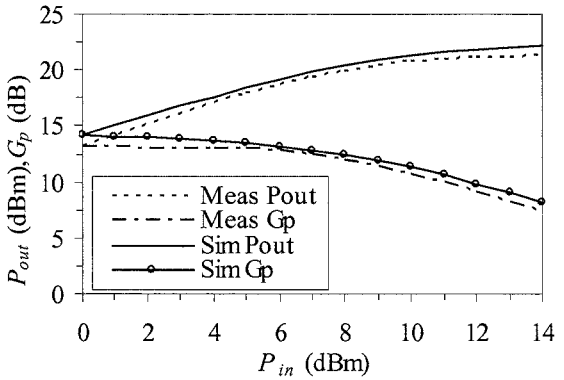


Figure 5.34: Simulated and measured G_p and P_{out} as a function of P_{in} at 2.45 GHz.

For an 8 dBm P_{in}, which corresponds to a 1 dB-compression, the measured PAE is 64% and the P_{out} is 19.9 dBm. When the value of P_{in} is increased to 11 dBm the active device is driven into saturation, the measured P_{out} is 21 dBm and the PAE increases to a peak of 70.4%. Again a good agreement between the simulated and measured results is obtained. The simulated PAE is slightly higher than the measured result.

Simulated and measured responses for the PAE, P_{out} and G_p as a function of frequency are shown in Figures 5.35 and 5.36. In the frequency range 2.05-2.52 GHz a PAE of over 60% and a P_{out} above 19.5 dBm have been obtained.

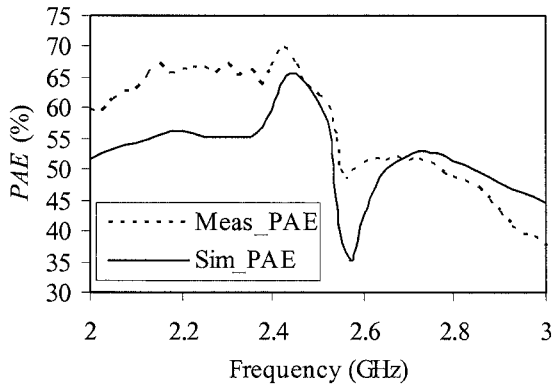


Figure 5.35: Simulated and measured PAE as a function of frequency at P_{in}=9 dBm.

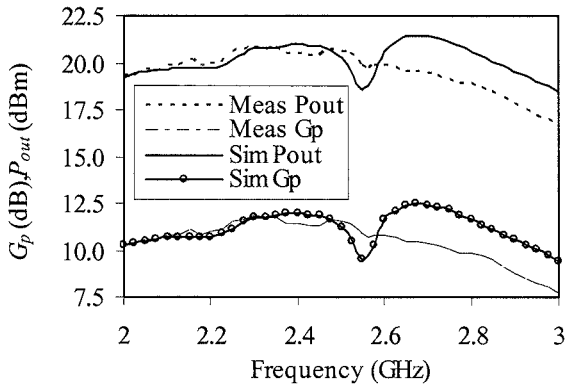


Figure 5.36: Simulated and measured G_p and P_{out} as a function of frequency at P_{in}=9 dBm

5.7 Summary

At higher frequencies the nonlinearity of the gate capacitance degrades the efficiency of a PA and therefore both source and load harmonic matching networks are needed to ensure maximum efficiency is obtained. Two new proposed harmonic matching networks have been designed, one for the first two harmonics and one for the first three harmonics.

The measured peak PAE and PAE, drain efficiency, and, output power at the 1-dB compression point of the PAs are compared in Table 5.5. In the table PA_2H refers to the PA with matching for the first two harmonics and PA_3H refers to matching for the first three harmonics.

PA	Peak PAE (%)	$PAE_{\_1\text{-}dB}$ (%)	$\eta_{d\_1\text{-}dB}$ (%)	$P_{out\_1\text{-}dB}$ (dBm)
PA_2H (Section 5.4)	74.5	53.8	57.7	18.72
PA_3H (Section 5.6)	70.4	64	68.3	19.9

Table 5.5: Comparisons of PAs' performances in terms of measured PAE, η_d and P_{out}.

For the case of a lossless transmission line the PAE obtained for PA_3H is slightly higher than that for the PA_2H. However in practical realisation, Table 5.5 shows that the PA_2H produces a higher measured peak PAE at the saturation point than does the PA_3H. This is because the simple compact circuit PA_2H has smaller losses compared to the PA_3H. However, the drawback of this topology is that matching is designed only up to the second harmonic and hence compared to the PA_3H there is a poorer suppression of the third harmonic output power. This topology is useful for applications where linearity is not a major concern.

On the other hand, the PA_3H gave a better performance at the 1-dB compression point, with a 64% PAE and a more than 68% drain efficiency and better linearity compared with the PA_2H. The benefit of the harmonic matching networks is that the impedance can be controlled at each harmonic but at the expense of additional components, and, also losses can increase. These losses result in the simulated and measured peak PAE for the PA_3H being 3% and 4% lower than that for the PA_2H. However the two PAs produced a PAE greater than 70% and good agreement was obtained between the simulated and measured results.

In Table 5.6 and Figure 5.37 the measured results obtained from this work are compared with the published results for class-F PAs with load and source harmonic matching networks.

Reference	V_{dd} (V)	f_1 (GHz)	PAE (%)	P_{out} (dBm)
[84]	3.5	0.93	74	31.4
[85]	5	1.8	71	42
[29]	5	5	60	25.6
[37]	3	2	76	20.9
This work (Section 5.4)	3	2.45	74.5	21.21
This work [36] (Section 5.6)	3	2.45	70.4	21

Table 5.6: Performances of GaAs FET class-F PAs with source/load matching networks.

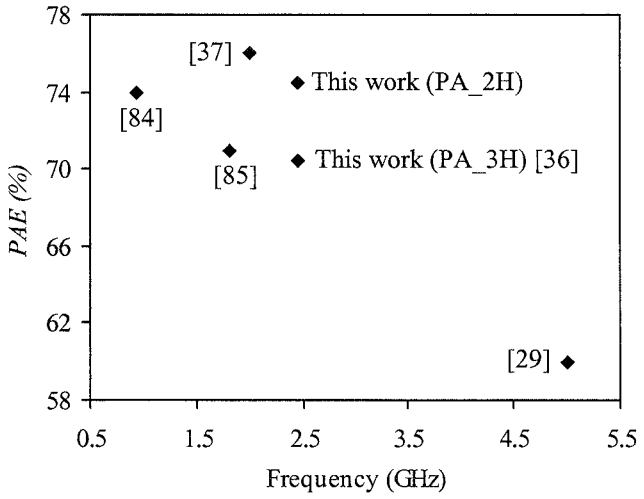


Figure 5.37: PAE of GaAs FET class-F PAs with source/load matching networks.

As can be seen the PAE obtained in this work is comparable with the results reported in other published papers. From Figure 5.37 it can be seen that the PAE for the GaAs FET class-F PA, designed using load and source harmonic matching networks, is above 70% in the frequency range below 3 GHz. This is significantly better than that obtained using only a load harmonic matching network.

CHAPTER 6 REVIEW OF MICROSTRIP PATCH ANTENNAS AND COUPLING IMPEDANCE FORMULAS FOR A RECTANGULAR PATCH

6.1 Introduction

A microstrip patch antenna was first proposed in 1953 [88] but it was not until the late 1970s that the many advantages of this antenna were appreciated. These antennas were subsequently used in both the military field and in commercial applications. The commercial applications include personal communications systems (PCS), mobile satellite communications, and, wireless local area networks (WLANs). This chapter briefly reviews the basic properties, feed methods and electrical models that are used in the design of patch antennas.

In Section 6.2 a brief review of the basic characteristics and a literature review of microstrip patch antennas are given. Their advantages and disadvantages are also discussed. In Section 6.3 the four most common feed methods and their advantages and disadvantages are presented. In Section 6.4 there is a brief outline of the three most used antenna models: transmission-line [89], cavity [90], and, full-wave [91]. Explicit efficient perimeter port coupling impedance formulas for a rectangular patch are given in Section 6.5 [92].

6.2 Basic Characteristics and Literature Review of Microstrip Patch Antennas

Microstrip patch antennas are widely used in today's wireless communication systems. Two of the most important requirements for these systems are small size and wide bandwidth. In the case of transmitters it is also necessary to design the antenna so that it has optimum input impedances at one or more harmonics in order to produce a high efficiency performance. This active integrated antenna (AIA) approach enables a compact

transmitter to be designed. A review of the research works carried out using different approaches to obtain size reduction and to design AIA circuits is presented in this section.

A microstrip patch antenna shown in Figure 6.1 consists of a very thin metallic patch separated from the ground plane by a dielectric substrate with dielectric constant, ϵ_r. The radiation from the antenna is produced by the horizontal components of the fringing electric fields in the two slots at two opposite edges of the antenna.

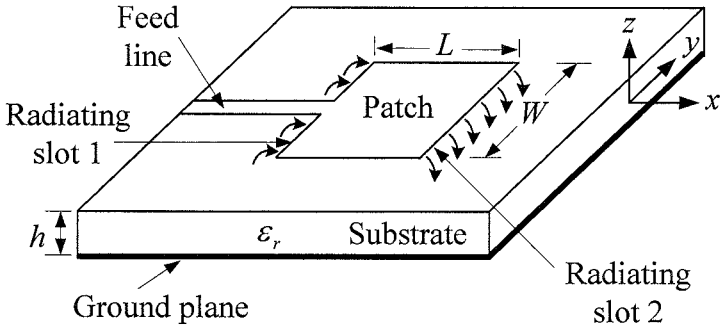


Figure 6.1: Microstrip patch antenna structure.

The physical length, L and width, W of the patch determine the frequency and the input impedance at the fundamental mode. To obtain a wide impedance bandwidth a thick dielectric substrate having a low dielectric constant should be used. However, as the thickness h of the substrate increases so does the dielectric loss and hence the efficiency of the antenna is reduced. Consequently, if a wide bandwidth is required an air substrate is used and the patch is supported by plastic screws. This type of structure is expensive to fabricate.

Microstrip patch antennas have the following advantages as compared with other forms of microwave antennas (horn antennas, reflector antennas, travelling wave antennas). They are lightweight, compact, and, inexpensive to manufacture. Their planar natures and low profile makes them ideal for use on satellites and missiles. Also they can easily be integrated with microwave and millimetre-wave circuits such as in power

amplifiers (PAs), low-noise amplifiers (LNAs), oscillators, mixers, and, multipliers. Further, as the feed lines and matching networks are on the same substrate as the antenna the manufacturing processes is simple and hence inexpensive. The main disadvantages of microstrip patch antennas are their narrow bandwidth, low gain and poor isolation between the feed and the radiating elements.

The design of compact microstrip patch antennas has received much attention as there is an increasing demand for small antennas to be used in personal communications systems such as cell phones and laptops. One of the simplest ways to produce a compact antenna is to use a high dielectric constant substrate [93]. However, the use of this substrate increases the cost of production.

Another approach to reduce the overall size of the antenna is to terminate one of the radiating edges with a short circuit. This short circuit can be in the form of a metal clamper or a series of shorting pins. In [94]-[96], shorting pins were used in different arrangements to reduce the overall size of the antennas. The drawback of this method is that as the shorting pins have to be accurately inserted into the substrate in specific positions the fabrication becomes more complex and hence more expensive.

Another strategy is to modify the geometry of a planar antenna so that it occupies less area than the conventional rectangular patch. This can be done by etching rectangular, square or triangular slots on the patch [97]-[99]. With this modification, the surface current path length on the patch is increased and hence the resonant frequency is reduced. The slot-loaded antennas include the C-shaped patch [97], H-shaped patch [98], rectangular ring patch [98], and, bowtie patch [99]. However, these antennas have a narrow impedance bandwidth. The design of a compact H-shaped patch antenna is discussed in detail in the Chapter 8 and the antenna is applied in Chapter 9 in AIA circuit design.

Another design approach to produce a compact antenna is to use a slot in the ground plane to increase the patch surface current path length which produces a small

improvement in the impedance bandwidth [100]. In [101], slits were etched on both the patch and ground plane which resulted in a further reduction in the size of the antenna. However, the main disadvantage of the two designs is that the slots in the ground plane produce backward radiations.

Another approach to minimise the antenna size is to use an open square ring antenna [102]. Although a smaller size antenna was obtained the impedance bandwidth was reduced and there was an increase in the cross-polarisation radiation in the both E- and H-planes.

The research has also concentrated on the integration between an antenna with an active device to produce an AIA circuit. The AIA designs are normally classified into three basic types depending on the function of the active device. There are oscillator-type AIA, frequency conversion-type AIA, and, amplifier-type AIA [2].

For the oscillator-type AIA, the oscillator and the antenna are integrated together and the antenna not only acts as a radiation element but as a positive feedback element for the active device [103]. This approach reduces the size, cost and losses of the combined unit. Recently, an oscillator-type AIA using a T-shaped microstrip coupled patch antenna has been reported [104]. In this design the antenna is used as a radiator, feedback element and a dc isolator for the ac signals so that the dc block capacitors are eliminated at the drain terminals.

The second group is the frequency conversion-type AIA. In [105] a design is presented for a frequency doubler where at the fundamental frequency the antenna acts as a radiator and a reflector. This type of antenna replaces a quarter-wave length open circuit stub which is normally used.

For the amplifier-type AIA, the antenna is connected directly either to the input of the active device (receiver) [106], or, to output of the active device (transmitter) [107]. In [106], the antenna was used to obtain the optimum source impedance for a LNA so that the

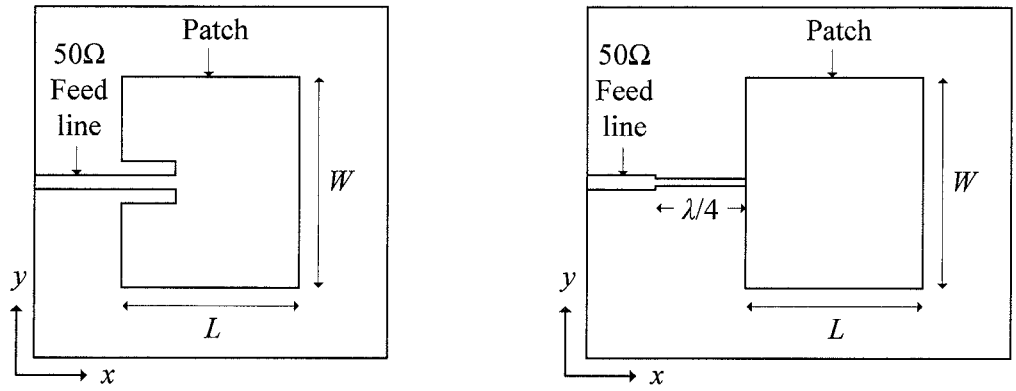
matching network between the antenna and LNA was eliminated. The size of the receiver module was reduced and as the losses were also reduced so a higher gain was obtained. In transmitter design [107], a circular sector patch antenna was used both as a radiator and a harmonic tuning circuit to produce a high efficiency compact AIA. The increase in efficiency was obtained by the lower losses. Designs of amplifier-type AIA are presented in Chapter 9.

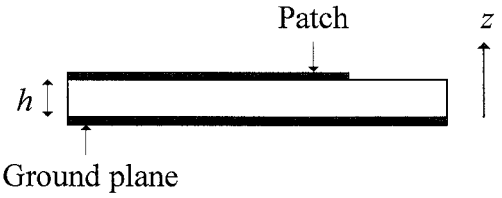
6.3 Review of Feed Methods for Microstrip Patch Antennas

The two common direct feed methods are the microstrip-line feed and the coaxial probe feed [89] while the aperture-coupled feed [108] and the proximity-coupled feed [109] are indirect feed methods. The advantages and disadvantages of each feed method are discussed below.

6.3.1 Microstrip-line feed

The microstrip-line feed (see Figure 6.1) is the simplest and easiest feed to fabricate. Large planar arrays are normally fabricated using this method. Matching of the antenna to 50 Ω is obtained using either an inset feed (see Figure 6.2(a)), or, a quarter-wave transformer (see Figure 6.2(b)).





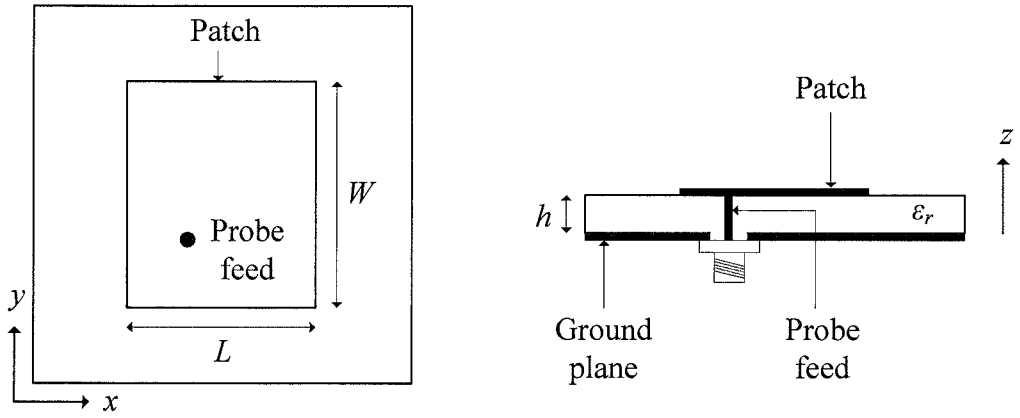
(c)

Figure 6.2: Microstrip-line feed patch antenna. (a) Inset feed. (b) Quarter-wave transformer. (c) Side view.

For this type of feed method there is a conflict in the choice of the dielectric constant of the substrate. For high radiation efficiency dielectric constant should be low. However, to reduce spurious radiation from the feed line, the width of the line should be narrow and hence high value of dielectric constant should be used which results in the antenna having a narrow impedance bandwidth.

6.3.2 Coaxial probe feed

Another form of direct feed method is the probe feed method as shown in Figure 6.3. In order to produce matching the feed location needs to be carefully selected.



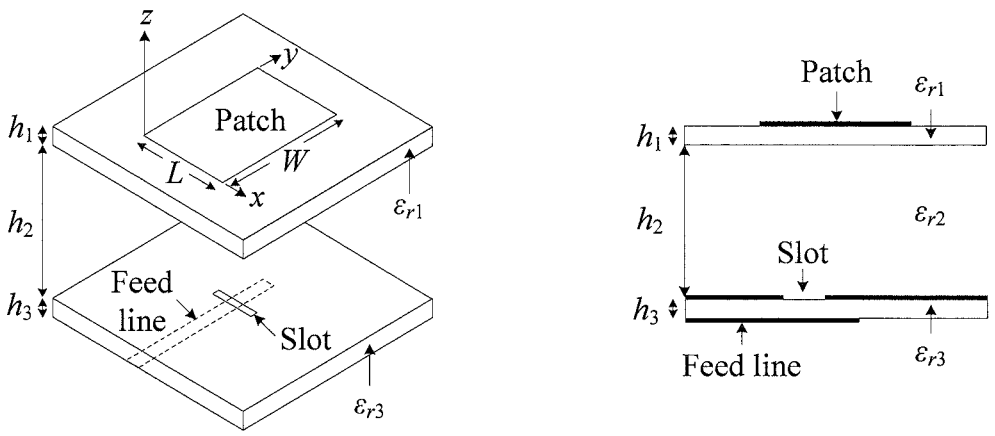
(a) (b)

Figure 6.3: Coaxial probe feed patch antenna. (a) Top view. (b) Side view.

The advantage of a coaxial probe feed as compared with a microstrip-line feed is that it has low spurious radiation since the probe is isolated from the patch. However for a probe feed the manufacturing is more complicated. Both the microstrip-line feed, and, the coaxial probe feed have a narrow bandwidth and generate higher order modes which produce cross-polarised radiation. To overcome these problems, aperture- and proximity-coupled feeds can be used.

6.3.3 Aperture-coupled feed

The aperture-coupled feed method was first proposed by Pozar [108] and uses two substrates separated by an air gap, as shown in Figure 6.4.



(a) (b)

Figure 6.4: Aperture-coupled feed patch antenna. (a) Top view. (b) Side view.

On the lower substrate there is a microstrip feed line which couples the energy to the patch through a slot on the ground plane separating the two substrates. This significantly reduces the spurious radiation from the feed network as the feed line is behind the ground plane. Further ϵ_{r3} is normally high and h_3 is normally small so that a narrow feed line width is used for the microstrip line to reduce spurious radiation from the microstrip feed line. The substrate above the ground plane has a large value of h_2, and, a low ϵ_{r2} so that a wide

bandwidth can be obtained. The patch substrate (ϵ_{r1}) is simply used to support the antenna and has a negligible effect on the performance of the antenna at frequencies below 8 GHz.

With the coupling aperture located at the centre beneath the patch the cross-polarised radiation is also reduced. Another advantage of this feed method compared to the direct feed methods is that it allows independent optimisation of the feed and antenna substrates. Also, since the aperture-coupled patch has more design parameters than the direct contact fed patches it is possible to produce a trade-off between return loss and its bandwidth.

However, alignment between the patch, slot and feed network is very critical and also a multilevel fabrication process is typically required. It is also difficult to fabricate the large air gap.

6.3.4 Proximity-coupled feed

The second form of indirect feed method, which is also proposed by Pozar [109] is the proximity-coupled method as shown in Figure 6.5.

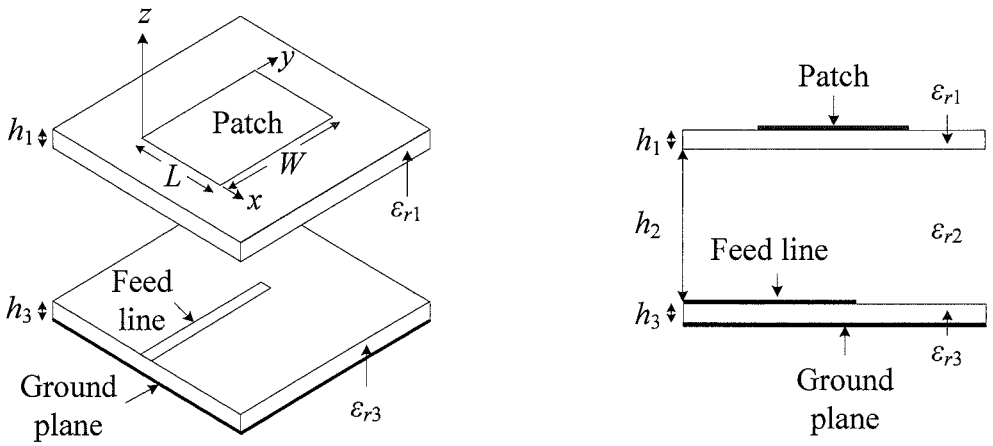


Figure 6.5: Proximity-coupled feed patch antenna. (a) Top view. (b) Side view.

The proximity-coupled feed uses three layers of substrates. The microstrip-line feed network is on the substrate (ϵ_{r3}) immediately above the ground plane and the top substrate

(ϵ_{r1}) supports the patch. The middle substrate (ϵ_{r2}) is normally air so that a wide impedance bandwidth is obtained. In proximity coupling the coupling mechanism is capacitive and hence even produces a wider bandwidth compared to the direct feed methods. The feed line radiation is very low as there are no slots in the ground plane. However, as in the case of the aperture-coupled antennas the same fabrication difficulties are present. An L-shape probe feed is used [110] as shown in Figure 6.6. The horizontal part of the L-shape produces increased capacitive coupling resulting in a wider impedance bandwidth.

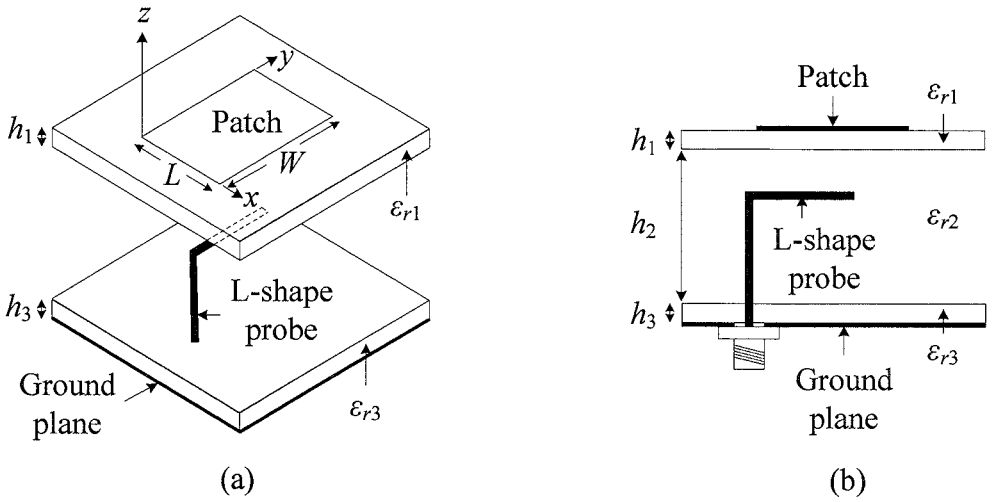


Figure 6.6: L-shape probe feed patch antenna. (a) Top view. (b) Side view.

6.4 Microstrip Antenna Modelling

In this section the most frequently used models of microstrip antennas, the transmission-line [89], cavity [90] and full-wave [91], are discussed below.

6.4.1 Transmission-line model

The transmission-line model is a simple model and gives good physical and engineering understanding of the properties of a rectangular patch antenna. However, this model has the following disadvantages. This model is normally used only for a rectangular antenna as it is very difficult to use this model for other shapes of antennas. Also this

model is not able to accurately model the effect of the electric fringing fields along the radiation edges: the fringing field along the other two edges of the patch are negligible. Hence this model is used for applications where an approximate result is required.

Figure 6.7(a) shows the electric fringing fields along the radiating edges of a rectangular patch which are represented by two radiating slots. L_e is the effective length, L is the physical length of the patch and ΔL is the length of the radiating slot. In the design L_e is a half wavelength at the design frequency while ΔL can be obtained from an empirical equation. The equivalent circuit of the centre feed rectangular patch antenna is shown in Figure 6.7(b) where the two slots are modelled as parallel circuits connected by a transmission line. The radiated power at each edge is modelled by the conductance G_1 and the power lost due to the coupling between the two slots by G_{12} [111]. The electrical length extensions due to the two slots are modelled as two capacitors having susceptance B_1.

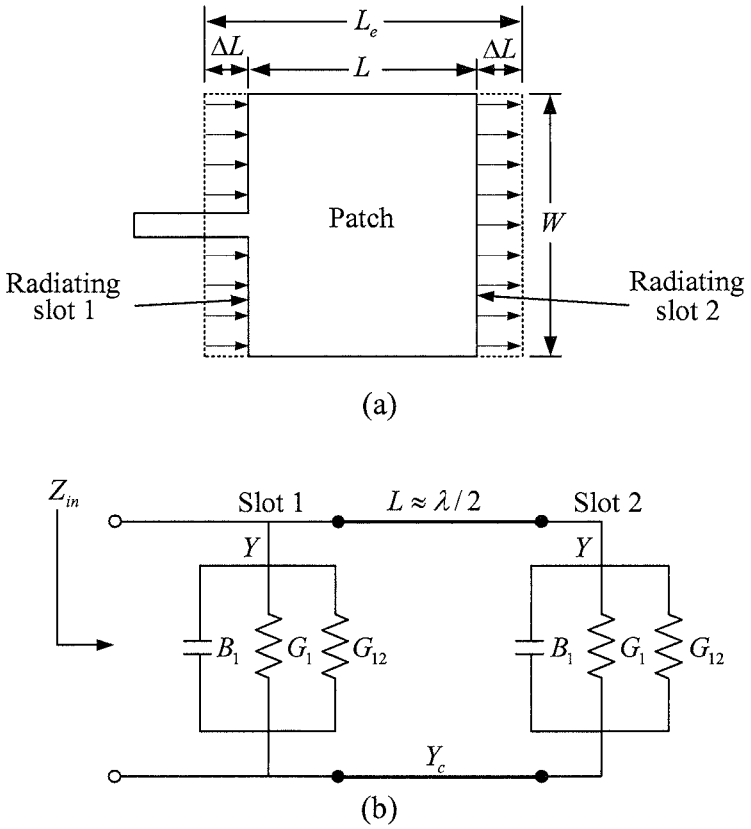


Figure 6.7: (a) Rectangular patch. (b) Transmission-line model equivalent circuit.

As the physical length L is slightly less than $\lambda/2$ the resonant input impedance for the TM_{10} mode is given

$$Z_{in} = R_{in} = \frac{1}{2(G_1 \pm G_{12})} \tag{6.1}$$

where, the (+) sign corresponds to the odd modes and the (−) sign to the even modes. The conductances G_1 and G_{12} can be obtained from the following equations given in [112].

The conductance G_1 is given by

$$G_1 = \frac{2P_{rad}}{|V_0|^2} \tag{6.2}$$

The radiated power given by

$$P_{rad} = \frac{|V_0|^2}{2\pi\eta_0} \int_0^{\pi} \left[\frac{\sin\left(\frac{k_0 W}{2}\cos\theta\right)}{\cos\theta} \right]^2 \sin^3\theta \, d\theta \tag{6.3}$$

where, V_0 is the voltage across the slot.

The mutual conductance G_{12} is given by [111]

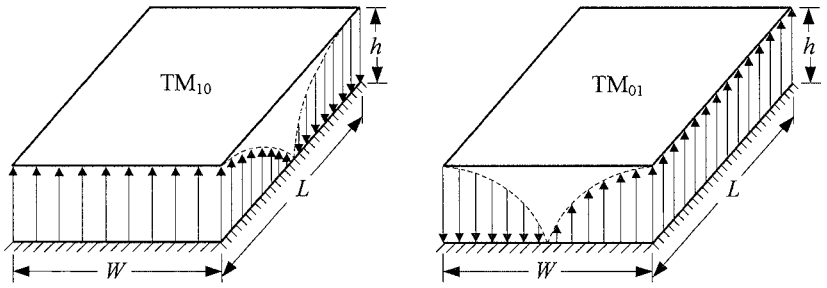
$$G_{12} = \frac{1}{120\pi^2} \int_0^{\pi} \left[\frac{\sin\left(\frac{k_0 W}{2}\cos\theta\right)}{\cos\theta} \right]^2 J_0(k_0 L \sin\theta) \sin^3\theta \, d\theta \tag{6.4}$$

where, J_0 is the order zero Bessel function of the first kind.

The transmission-line model was original developed for rectangular patches but has been extended to more general patch shapes such as the bowtie [113], [114]. A transmission-line model has also been used in the modelling of a wide bandwidth slot-coupled rectangular patch antenna where different substrates are used for the feed network and the patch [115].

6.4.2 Cavity model

In the cavity model, the region between the patch and the ground plane is considered as a cavity bounded by four vertical magnetic walls and, electric walls on the patch and ground plane [90]. If the thickness of the substrate is much less than a wavelength the electric field inside the cavity is uniform in the z direction. The model fields TM_{10}, TM_{01} on the cavity walls are shown in Figure 6.8, below.



(a) (b)

Figure 6.8: Field configurations for rectangular patch. (a) TM_{10} mode. (b) TM_{01} mode.

Applying the magnetic wall boundary conditions the wavenumber components are given by [112]

$$k_x = m\pi / L_e,\ k_y = n\pi / W_e, \tag{6.5}$$

where, L_e and W_e are the effective dimensions of the patch and

$$k_x^2 + k_y^2 = \left(\frac{m\pi}{L_e}\right)^2 + \left(\frac{n\pi}{W_e}\right)^2 = k_{m,n}^2 = \omega^2\mu\varepsilon = \omega^2\mu_0\varepsilon_0\varepsilon_{reff} \tag{6.6}$$

where, m=0, 1, 2,..., n=0, 1, 2,..., and $m = n \neq 0$.

The resonant frequencies for the TM_{mn} modes are given by

$$f_{mn} = \frac{c_0}{2\pi\sqrt{\varepsilon_{reff}}}\sqrt{\left(\frac{m\pi}{L_e}\right)^2 + \left(\frac{n\pi}{W_e}\right)^2} \tag{6.7}$$

and, the TM_{10} and TM_{01} are given by

$$f_{10} = \frac{c_0}{2L_e\sqrt{\varepsilon_{reff}}}. \tag{6.8a}$$

and,

$$f_{01} = \frac{c_0}{2W_e\sqrt{\varepsilon_{reff}}}. \tag{6.8b}$$

A modified Wolf model was proposed in [116] to compute a more accurate value of the resonant frequency for a rectangular patch antenna with a thick substrate. Zhang and Wang [117] suggested an improved cavity model to obtain the input impedance of a differentially driven rectangular antenna which is used in efficient active PAs.

6.4.3 Full-wave model

In the full-wave model the electric current density distribution on the patch conductor is used to determine the mode frequencies. This model maintains rigor and accuracy at the expense of computational simplicity. The principle assumption is that the substrate and ground plane are infinite in lateral dimensions, so that no fringing field is considered. The formulation of the solution is based on rigorously enforcing the boundary conditions at the air-dielectric interface. This is done using the Green's function for the composite dielectric [114], [118].

The boundary condition at the patch produces an integral equation of the form

$$E(x,y) = \int_{S(x,y)} G\,J(x,y)\,dx\,dy \tag{6.9}$$

where, $J(x, y)$ is the current density on the patch.

This equation is solved using the method of moments (MoM) by taking $J(x, y)$ in the expanded form

$$J(x,y) = \sum_{n=1}^{\infty} c_n\,J_n(x,y) \tag{6.10}$$

where, $J_n(x, y)$ are a chosen set of basis functions, and, c_n are the expansion coefficients obtained by solving the above integral equation.

In a purely numerical approach the finite difference time domain (FDTD) method given in [119] Maxwell's equations are replaced by their finite difference approximations. The infinite space is replaced by a finite enclosed absorbing boundary on which conditions are imposed emulating the conditions at infinity so there are no reflected waves [119], [120]. An initial field is injected into the antenna structure and the difference equations solved for the fields throughout the space domain for each time step until a steady state is obtained. The electric current distributions at all points on the difference grid on the conducting element can then be obtained from which all the other parameters of interest can be derived.

6.5 Perimeter Coupling Impedance Formulas on a Rectangular Patch

The coupling impedance formulas are based on coplanar circuit analysis [121] which is discussed in Chapter 7 where it is shown that the coupling impedance between two ports on a microstrip patch is given by

$$Z_{pq} = \frac{1}{W_p W_q} \int_{W_p} \int_{W_q} G(x_p, y_p \mid x_q, y_q)\, dr_q\, dr_p \tag{6.11}$$

where, dr_p and dr_q are incremental distances over the port widths W_p, $W_q << \lambda$, [114], a condition for the assumption that the current density does not vary appreciably across the ports. G is the Green's function of the patch geometry.

Following the approach in Chapter 7 the following results were obtained.

Case A: Two ports on the same side

The two ports p and q, have widths W_p, W_q respectively, and are on the same side is shown in Figure 6.9.

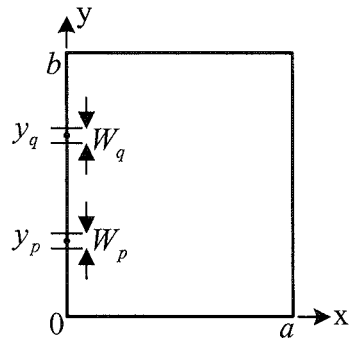


Figure 6.9: Rectangular segment with two ports on the same side.

For ports located at $(0, y_p)$, $(0, y_q)$ the Green's function is

$$G(0,y_p \mid 0,y_q) = \frac{j\omega\mu h}{ab}\left[-\frac{1}{k^2}+\frac{2a^2}{\pi^2}\sum_{m=1}^{\infty}\frac{1}{m^2-A^2}+\frac{2b^2}{\pi^2}\sum_{n=1}^{\infty}\frac{\cos\frac{n\pi}{b}y_p\cos\frac{n\pi}{b}y_q}{n^2-B^2}\right.$$

$$\left.+\frac{4}{\pi^2}\sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\frac{\cos\frac{n\pi}{b}y_p\cos\frac{n\pi}{b}y_q}{\frac{m^2}{a^2}+\frac{n^2}{b^2}-\frac{k^2}{\pi^2}}\right] \tag{6.12}$$

where, $A=ak/\pi$ and $B=bk/\pi$,

and, the coupling impedance is given by

$$Z_{pq} = \frac{1}{W_p W_q}\int_{W_p}\int_{W_q} G(0,y_p \mid 0,y_q)\, dy_q\, dy_p \tag{6.13}$$

By integration, and using the closed form summations [122] the economised coupling impedance formula is given by [92]

$$Z_{pq} = j\omega\mu h\left[-\frac{\cot ak}{bk}\right.$$

$$\left.+\frac{2b^2}{W_p W_q \pi^3}\sum_{n=1}^{\infty}\frac{(\sin n\theta_1-\sin n\theta_2)(\sin n\theta_3-\sin n\theta_4)}{n^2\sqrt{n^2-B^2}}\coth\frac{a\pi}{b}\sqrt{n^2-B^2}\right] \tag{6.14}$$

where, $\theta_1 = \frac{\pi}{b}\left(y_p+\frac{W_p}{2}\right)$; $\theta_2 = \frac{\pi}{b}\left(y_p-\frac{W_p}{2}\right)$; $\theta_3 = \frac{\pi}{b}\left(y_q+\frac{W_q}{2}\right)$; $\theta_4 = \frac{\pi}{b}\left(y_q-\frac{W_q}{2}\right)$.

The coupling impedance Z_{pq} is obtained in terms of a closed form and a single infinite series.

For a rectangular patch antenna the input, or, self impedance for a microstrip feed is obtained from the equation (6.14) by taking $q=p$, $\theta_3=\theta_1$, and, $\theta_4=\theta_2$. The economised input impedance formula is then given by

$$Z_{pp} = Z_{in} = j\omega\mu h\left[-\frac{\cot ak}{bk}+\frac{2b^2}{W_p{}^2\pi^3}\sum_{n=1}^{\infty}\frac{(\sin n\theta_1-\sin n\theta_2)^2}{n^2\sqrt{n^2-B^2}}\coth\frac{a\pi}{b}\sqrt{n^2-B^2}\right]. \tag{6.15}$$

The perimeter port input impedance Z_{pp} is obtained in terms of a closed form and a single infinite series.

Case B: Two ports on adjacent sides

The port configuration is shown in Figure 6.10.

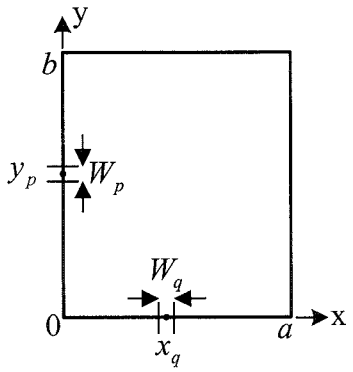


Figure 6.10: Rectangular segment with two ports on adjacent sides.

The economised coupling impedance formula is given by

$$Z_{pq} = j\omega\mu h\left[\frac{\sin A(\pi-\theta_4)-\sin A(\pi-\theta_3)}{bk^2W_q\sin ak}+\frac{2b^2}{W_pW_q\pi^3}\right.$$

$$\left.\cdot\sum_{n=1}^{\infty}\frac{(\sin n\theta_1-\sin n\theta_2)\left[\sinh\frac{a(\pi-\theta_3)}{b}\sqrt{n^2-B^2}-\sinh\frac{a(\pi-\theta_4)}{b}\sqrt{n^2-B^2}\right]}{n(n^2-B^2)\sinh\frac{a\pi}{b}\sqrt{n^2-B^2}}\right] \tag{6.16}$$

where, $\theta_1=\frac{\pi}{b}\left(y_p+\frac{W_p}{2}\right);\theta_2=\frac{\pi}{b}\left(y_p-\frac{W_p}{2}\right);\theta_3=\frac{\pi}{a}\left(x_q+\frac{W_q}{2}\right);\ \theta_4=\frac{\pi}{a}\left(x_q-\frac{W_q}{2}\right).$

The coupling impedance Z_{pq} is obtained in terms of two closed forms, and, a single infinite series.

Case C: Two ports on opposite sides

The port configuration is shown in Figure 6.11.

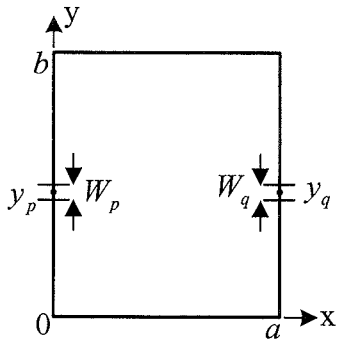


Figure 6.11: Rectangular segment with two ports on opposite sides.

The economised coupling impedance formula is given by

$$Z_{pq} = j\omega\mu h\left[\frac{1}{bk\sin ak} - \frac{2b^2}{W_p W_q \pi^3}\sum_{n=1}^{\infty}\frac{(\sin n\theta_1 - \sin n\theta_2)(\sin n\theta_3 - \sin n\theta_4)}{n^2\sqrt{n^2 - B^2}\,\sinh\frac{a\pi}{b}\sqrt{n^2 - B^2}}\right] \tag{6.17}$$

where, $\theta_1 = \frac{\pi}{b}\left(y_p + \frac{W_p}{2}\right)$; $\theta_2 = \frac{\pi}{b}\left(y_p - \frac{W_p}{2}\right)$; $\theta_3 = \frac{\pi}{b}\left(y_q + \frac{W_q}{2}\right)$; $\theta_4 = \frac{\pi}{b}\left(y_q - \frac{W_q}{2}\right)$.

The coupling impedance Z_{pq} is obtained in terms of a closed form and a single infinite series.

6.6 Summary

Reviews of the basic characteristics, feed methods and modelling of a microstrip patch antenna have been presented. The advantages and disadvantages of different feed

methods were given. Recent trends on designing compact size microstrip patch antennas and multifunctional patch antennas for AIA design have been discussed.

Explicit efficient coupling impedance formulas for the microstrip feed rectangular patch antenna are given. These coupling impedances together with the new derived coupling impedance formulas for probe feed rectangular patch antenna (see Chapter 7) are then applied to evaluate the elements in matrix input impedance formula for the H-shaped patch antenna presented in Chapter 8.

CHAPTER 7 NEW PROBE FEED IMPEDANCE FORMULAS FOR A RECTANGULAR PATCH ANTENNA

7.1 Introduction

A computationally efficient general coupling impedance formula for ports on a rectangle is derived in [123]. This was derived by first reducing the double series Green's function to a single series, using a closed form of Fourier series prior to the integration step. In application it is necessary to employ several complicated selection rules. However, as reported, for large values of the complex arguments in the trigonometric functions numerical convergence problems arise and at this point in the series these functions had to be replaced by their large argument approximations.

New explicit computationally efficient probe feed coupling impedance formulas are presented in this chapter. In each case the Green's functions are first partitioned and the integration is performed prior to the introduction of closed forms of infinite series [122]. This procedure facilitates the identification of both the single terms and the infinite series terms which cancel each other out and this is primarily due to the initial partitioning. No problems arise with large values of the arguments in the trigonometric functions [92], [124].

The cavity model is used, in which, to account for the fringing fields the patch geometry is extended outwards to a magnetic wall where the outward normal voltage gradient is zero [121]. For a thin substrate ($h<<\lambda$) [114] it is assumed that the electric and magnetic fields do not vary in the z-direction, so that the antenna may be modelled as a two dimensional structure. For this structure coplanar circuit analysis [121] may be used to derive coupling impedance formulas. A new explicit computationally efficient probe self impedance formula, and, a formula for the coupling impedance between the probe and a perimeter port on a rectangular patch are derived in Section 7.3 [125]. These coupling

impedance formulas are then applied in Chapter 8 for evaluating the input impedance of an H-shaped patch antenna. This work has been published in [125].

7.2 Coplanar Circuit Analysis

An arbitrary shaped microstrip patch antenna with a probe feed is shown in Figure 7.1, where the origin of coordinates is located on the ground plane.

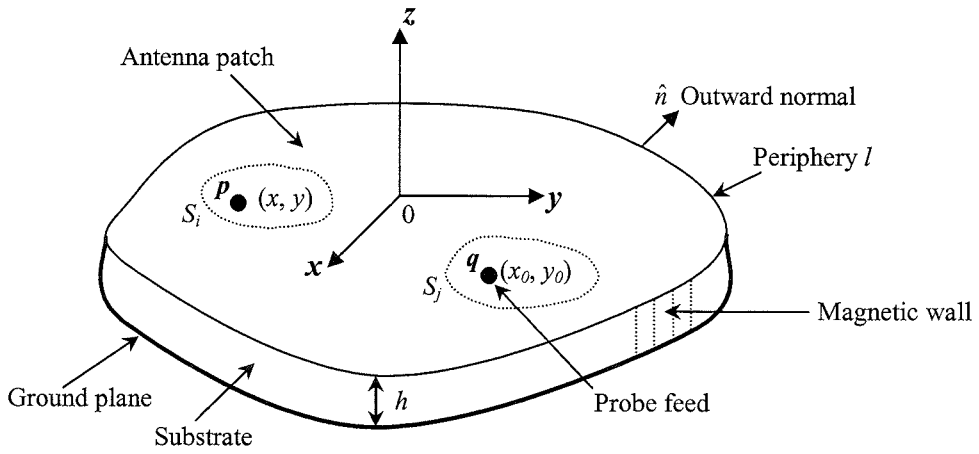


Figure 7.1: Antenna structure with a probe feed.

For this structure the two dimensional non homogeneous voltage wave equation can be solved using the eigenfunction expansion method [126], [127] to show that the patch voltage $V(x, y)$ at the port p due to a current source density $J(x_0, y_0)$ at the port q is given by [121]

$$V(x,y) = \int_{S_j} G(x,y \mid x_0,y_0) J(x_0,y_0) dx_0\, dy_0 \tag{7.1}$$

where, $G(x, y \mid x_0, y_0)$ is the Green's function for the patch geometry.

A "terminal voltage" V_i on the segment S_i is defined as the average voltage over the port area S_i, so that

$$V_i = \frac{1}{S_i}\int_{S_i} V(x,y)\,dx\,dy\,. \tag{7.2}$$

Substituting $V(x, y)$ from equation (7.1) into equation (7.2) gives

$$V_i = \frac{1}{S_i}\int_{S_i}\int_{S_j} G(x,y|x_0,y_0)J(x_0,y_0)\,dx\,dy\,dx_0dy_0\,. \tag{7.3}$$

In applications the areas S_i, S_j of current sources are very small so that the current density $J(x_0, y_0)$ may be replaced by the average density I_j/S_j, where I_j is the total current through S_j. Substituting for $J(x_0, y_0)$ in equation (7.3) gives

$$V_i = \frac{1}{S_i}\int_{S_i}\int_{S_j} G(x,y|x_0,y_0)\frac{I_j}{S_j}\,dx\,dy\,dx_0dy_0$$

$$= \frac{I_j}{S_iS_j}\int_{S_i}\int_{S_j} G(x,y|x_0,y_0)\,dx\,dy\,dx_0dy_0\,. \tag{7.4}$$

The ratio V_i/I_j is defined as the coupling impedance Z_{ij} between the two ports hence,

$$Z_{ij} = \frac{1}{S_iS_j}\int_{S_i}\int_{S_j} G(x,y|x_0,y_0)\,dx\,dy\,dx_0dy_0\,. \tag{7.5}$$

In particular for a single feed the input, or, self impedance is, Z_{jj}.

7.3 New Explicit Coupling Impedance Formulas

The Green's function for a rectangular patch is given by [121]

$$G(x_p,y_p\,|\,x_q,y_q) = \frac{j\omega\mu h}{ab}\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\varepsilon_m{}^2\varepsilon_n{}^2\,\frac{\cos\frac{m\pi}{a}x_p\,\cos\frac{n\pi}{b}y_p\,\cos\frac{m\pi}{a}x_q\,\cos\frac{n\pi}{b}y_q}{\left(\frac{m\pi}{a}\right)^2+\left(\frac{n\pi}{b}\right)^2-k^2} \tag{7.6}$$

where, $\omega=2\pi f$, h is the thickness of the dielectric substrate, $k^2 = \omega^2\,\mu\,\epsilon_0\,\epsilon_{reff}(1 - j/Q)$, Q is the total quality factor, and,

$$\varepsilon_m = \begin{cases} 1 & (\text{for } m=0) \\ \sqrt{2} & (\text{for } m\neq 0) \end{cases}, \quad \varepsilon_n = \begin{cases} 1 & (\text{for } n=0) \\ \sqrt{2} & (\text{for } n\neq 0) \end{cases}.$$

The Green's function used in this analysis is partitioned into the four modal sets [128], $(m = 0, n = 0)$, $(m \geq 1, n = 0)$, $(m = 0, n \geq 1)$, $(m \geq 1, n \geq 1)$, to obtain the following partitioned form of the Green's function.

$$G(x_p, y_p \mid x_q, y_q) = \frac{j\omega\mu h}{ab}\left[-\frac{1}{k^2} + \frac{2a^2}{\pi^2}\sum_{m=1}^{\infty}\frac{\cos\frac{m\pi}{a}x_p \cos\frac{m\pi}{a}x_q}{m^2 - A^2}\right.$$

$$+\frac{2b^2}{\pi^2}\sum_{n=1}^{\infty}\frac{\cos\frac{n\pi}{b}y_p \cos\frac{n\pi}{b}y_q}{n^2 - B^2}$$

$$\left.+\frac{4}{\pi^2}\sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\frac{\cos\frac{m\pi}{a}x_p \cos\frac{m\pi}{a}x_q \cos\frac{n\pi}{b}y_p \cos\frac{n\pi}{b}y_q}{\frac{m^2}{a^2} + \frac{n^2}{b^2} - \frac{k^2}{\pi^2}}\right] \tag{7.7}$$

where, $A=ak/\pi$ and $B=bk/\pi$.

7.3.1 Coupling impedance between a probe feed and an internal port

Figure 7.2 shows the locations of the probe feed port p and an internal port q.

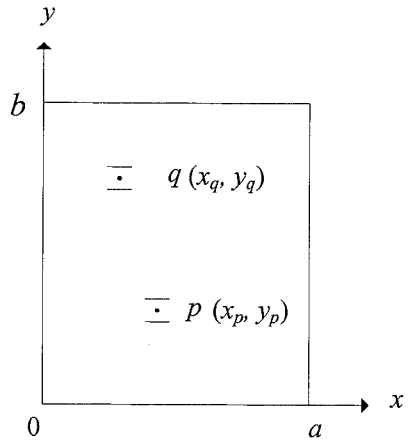


Figure 7.2: The locations of ports p and q.

The probe feed is replaced by a line feed in the y-direction of size equal to the probe diameter [118]. The coupling impedance, Z_{pq}, between the ports p and q is then

$$Z_{pq} = \frac{1}{W_p W_q} \int_{W_p} \int_{W_q} G(x_p, y_p \mid x_q, y_q)\, dy_q\, dy_p \tag{7.8}$$

where, dy_p and dy_q are incremental distances over the port widths W_p, $W_q << \lambda$ [114], a condition that the current density does not vary appreciably across the ports.

Using the partitioned form of the Green's function the coupling impedance between the ports p and q is

$$Z_{pq} = \frac{j\omega\mu h}{abW_pW_q} \int_{y_p-W_p/2}^{y_p+W_p/2} \int_{y_q-W_q/2}^{y_q+W_q/2} \left\{ -\frac{1}{k^2} + \frac{2a^2}{\pi^2} \sum_{m=1}^{\infty} \frac{\cos\frac{m\pi}{a}x_p \cos\frac{m\pi}{a}x_q}{m^2 - A^2} \right.$$

$$+ \frac{2b^2}{\pi^2} \sum_{n=1}^{\infty} \frac{\cos\frac{n\pi}{b}y_p \cos\frac{n\pi}{b}y_q}{n^2 - B^2}$$

$$\left. + \frac{4}{\pi^2} \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} \frac{\cos\frac{m\pi}{a}x_p \cos\frac{m\pi}{a}x_q \cos\frac{n\pi}{b}y_p \cos\frac{n\pi}{b}y_q}{\frac{m^2}{a^2} + \frac{n^2}{b^2} - \frac{k^2}{\pi^2}} \right\} dy_q\, dy_p . \tag{7.9}$$

Integration for first term

$$-\frac{1}{k^2} \int_{y_p-W_p/2}^{y_p+W_p/2} \int_{y_q-W_q/2}^{y_q+W_q/2} 1\, dy_q\, dy_p = -\frac{W_pW_q}{k^2} . \tag{7.10}$$

Integration for second term

$$\frac{2a^2}{\pi^2} \sum_{m=1}^{\infty} \frac{\cos\frac{m\pi}{a}x_p \cos\frac{m\pi}{a}x_q}{m^2 - A^2} \int_{y_p-W_p/2}^{y_p+W_p/2} \int_{y_q-W_q/2}^{y_q+W_q/2} 1\, dy_q\, dy_p = \frac{2a^2W_pW_q}{\pi^2} \sum_{m=1}^{\infty} \frac{\cos\frac{m\pi}{a}x_p \cos\frac{m\pi}{a}x_q}{m^2 - A^2} \tag{7.11}$$

Integration for third term

$$\frac{2b^2}{\pi^2} \sum_{n=1}^{\infty} \frac{1}{n^2 - B^2} \int_{y_p-W_p/2}^{y_p+W_p/2} \int_{y_q-W_q/2}^{y_q+W_q/2} \cos\frac{n\pi}{b}y_p \cos\frac{n\pi}{b}y_q\, dy_q\, dy_p \tag{7.12}$$

$$= \frac{2b^2}{\pi^2} \sum_{n=1}^{\infty} \frac{1}{n^2 - B^2} \frac{b^2}{n^2\pi^2} (\sin\theta_1 - \sin\theta_2)(\sin\theta_3 - \sin\theta_4) \tag{7.13}$$

$$= \frac{2b^4}{\pi^4} \sum_{n=1}^{\infty} \frac{(\sin n\theta_1 - \sin n\theta_2)(\sin n\theta_3 - \sin n\theta_4)}{n^2(n^2 - B^2)} \tag{7.14}$$

where, $\theta_1 = \frac{\pi}{b}\left(y_p + \frac{W_p}{2}\right)$; $\theta_2 = \frac{\pi}{b}\left(y_p - \frac{W_p}{2}\right)$; $\theta_3 = \frac{\pi}{b}\left(y_q + \frac{W_q}{2}\right)$; $\theta_4 = \frac{\pi}{b}\left(y_q - \frac{W_q}{2}\right)$.

Integration for fourth term

$$\frac{4}{\pi^2} \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} \frac{\cos\frac{m\pi}{a} x_p \cos\frac{m\pi}{a} x_q}{\frac{m^2}{a^2} + \frac{n^2}{b^2} - \frac{k^2}{\pi^2}} \int_{y_p - W_p/2}^{y_p + W_p/2} \int_{y_q - W_q/2}^{y_q + W_q/2} \cos\frac{n\pi}{b} y_p \cos\frac{n\pi}{b} y_q \, dy_q \, dy_p$$

$$= \frac{4b^2}{\pi^4} \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} \frac{\cos\frac{m\pi}{a} x_p \cos\frac{m\pi}{a} x_q (\sin n\theta_1 - \sin n\theta_2)(\sin n\theta_3 - \sin n\theta_4)}{n^2\left(\frac{m^2}{a^2} + \frac{n^2}{b^2} - \frac{k^2}{\pi^2}\right)}. \tag{7.15}$$

Substituting equations (7.10), (7.11), (7.13), (7.15) into (7.9) gives the following non economised formula for Z_{pq}.

$$Z_{pq} = \frac{j\omega\mu h}{abW_pW_q} \left\{ -\frac{W_pW_q}{k^2} + \frac{2a^2W_pW_q}{\pi^2} \sum_{m=1}^{\infty} \frac{\cos\frac{m\pi}{a} x_p \cos\frac{m\pi}{a} x_q}{m^2 - A^2} \right.$$

$$+ \frac{2b^4}{\pi^4} \sum_{n=1}^{\infty} \frac{(\sin n\theta_1 - \sin n\theta_2)(\sin n\theta_3 - \sin n\theta_4)}{n^2(n^2 - B^2)}$$

$$\left. + \frac{4b^2}{\pi^4} \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} \frac{\cos\frac{m\pi}{a} x_p \cos\frac{m\pi}{a} x_q (\sin n\theta_1 - \sin n\theta_2)(\sin n\theta_3 - \sin n\theta_4)}{n^2\left(\frac{m^2}{a^2} + \frac{n^2}{b^2} - \frac{k^2}{\pi^2}\right)} \right\}. \tag{7.16}$$

7.3.2 The probe feed to perimeter port coupling impedance

Figure 7.3 shows the q port at the perimeter of the rectangular segment, where x_q=0.

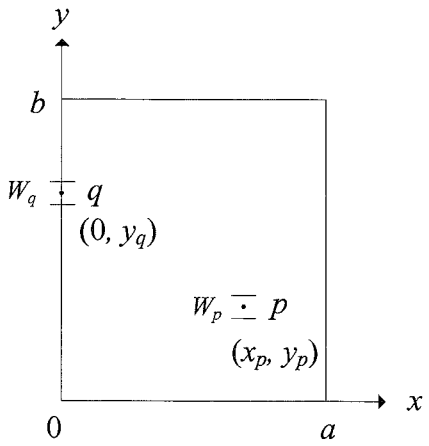


Figure 7.3: The locations of ports p and q where x_q=0.

Setting x_q=0 in equation (7.16) gives

$$Z_{pq} = \frac{j\omega\mu h}{abW_pW_q}\left\{-\frac{W_pW_q}{k^2}+\frac{2a^2W_pW_q}{\pi^2}\sum_{m=1}^{\infty}\frac{\cos\frac{m\pi}{a}x_p}{m^2-A^2}\right.$$

$$+\frac{2b^4}{\pi^4}\sum_{n=1}^{\infty}\frac{(\sin n\theta_1-\sin n\theta_2)(\sin n\theta_3-\sin n\theta_4)}{n^2(n^2-B^2)}$$

$$\left.+\frac{4b^2}{\pi^4}\sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\frac{\cos\frac{m\pi}{a}x_p(\sin n\theta_1-\sin n\theta_2)(\sin n\theta_3-\sin n\theta_4)}{n^2\left(\frac{m^2}{a^2}+\frac{n^2}{b^2}-\frac{k^2}{\pi^2}\right)}\right\}, \tag{7.17}$$

$$=\frac{j\omega\mu h}{abW_pW_q}\left\{-\frac{W_pW_q}{k^2}+\frac{2a^2W_pW_q}{\pi^2}\sum_{m=1}^{\infty}\frac{\cos\frac{m\pi}{a}x_p}{m^2-A^2}\right.$$

$$+\frac{2b^4}{\pi^4}\sum_{n=1}^{\infty}\frac{(\sin n\theta_1-\sin n\theta_2)(\sin n\theta_3-\sin n\theta_4)}{n^2(n^2-B^2)}$$

$$\left.+\frac{4a^2b^2}{\pi^4}\sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\frac{\cos\frac{m\pi}{a}x_p(\sin n\theta_1-\sin n\theta_2)(\sin n\theta_3-\sin n\theta_4)}{n^2(m^2+D^2)}\right\} \tag{7.18}$$

where, $\theta_1 = \frac{\pi}{b}\left(y_p + \frac{W_p}{2}\right)$; $\theta_2 = \frac{\pi}{b}\left(y_p - \frac{W_p}{2}\right)$; $\theta_3 = \frac{\pi}{b}\left(y_q + \frac{W_q}{2}\right)$; $\theta_4 = \frac{\pi}{b}\left(y_q - \frac{W_q}{2}\right)$,

$$D^2 = \frac{a^2n^2}{b^2} - \frac{a^2k^2}{\pi^2} = \frac{a^2}{b^2}\left(n^2 - \frac{b^2k^2}{\pi^2}\right) = \frac{a^2}{b^2}(n^2 - B^2).$$

In order to identify the terms in the above expression which cancel out, Z_{pq} is written in the following form

$$Z_{pq} = \frac{j\omega\mu h}{abW_pW_q}\left\{-\frac{W_pW_q}{k^2} + \frac{2a^2W_pW_q}{\pi^2}S_1(m) + \frac{2b^4}{\pi^4}S_2(n) + \frac{4a^2b^2}{\pi^4}S_3(m,n)\right\} \tag{7.19}$$

where, the infinite series $S_1(m)$, $S_2(n)$ and $S_3(m, n)$ are given below. The series $S_1(m)$ is reduced to a closed form, and the inner series in $S_3(m, n)$ on the index m has also been reduced to a closed form.

$$S_1(m) = \sum_{m=1}^{\infty} \frac{\cos\frac{m\pi}{a}x_p}{m^2 - A^2}$$

$$= \frac{1}{2A^2} - \frac{\pi\cos A\pi(1 - x_p/a)}{2A\sin A\pi}$$

$$= \frac{\pi^2}{2a^2k^2} - \frac{\pi^2\cos k(a - x_p)}{2ak\sin ak}, \tag{7.20}$$

$$S_2(n) = \sum_{n=1}^{\infty} \frac{(\sin n\theta_1 - \sin n\theta_2)(\sin n\theta_3 - \sin n\theta_4)}{n^2(n^2 - B^2)}, \tag{7.21}$$

$$S_3(m,n) = \sum_{n=1}^{\infty}\sum_{m=1}^{\infty} \frac{\cos\frac{m\pi}{a}x_p(\sin n\theta_1 - \sin n\theta_2)(\sin n\theta_3 - \sin n\theta_4)}{n^2(m^2 + D^2)}$$

$$= \sum_{n=1}^{\infty} \frac{(\sin n\theta_1 - \sin n\theta_2)(\sin n\theta_3 - \sin n\theta_4)}{n^2} \sum_{m=1}^{\infty} \frac{\cos m\frac{\pi x_p}{a}}{m^2 + D^2}$$

$$= \sum_{n=1}^{\infty} \frac{(\sin n\theta_1 - \sin n\theta_2)(\sin n\theta_3 - \sin n\theta_4)}{n^2} \left[\frac{\pi\cosh D\pi(1 - x_p/a)}{2D\sinh D\pi} - \frac{1}{2D^2}\right]$$

$$= \frac{b\pi}{2a}\sum_{n=1}^{\infty}\frac{(\sin n\theta_1 - \sin n\theta_2)(\sin n\theta_3 - \sin n\theta_4)\cosh\dfrac{(a-x_p)\pi}{b}\sqrt{n^2-B^2}}{n^2\sqrt{n^2-B^2}\sinh\dfrac{a\pi}{b}\sqrt{n^2-B^2}} - \frac{b^2}{2a^2}S_2(n). \qquad (7.22)$$

Substituting $S_1(m)$, and $S_3(m,n)$ from equations (7.20) and (7.22) respectively into (7.19) eliminates the terms $-W_pW_q/k^2$, and the infinite series $S_2(n)$. The double infinite series $S_3(m,n)$ has been reduced to single series form.

The new formula for Z_{pq} is then given by

$$Z_{pq} = j\omega\mu h\left\{-\frac{\cos k(a-x_p)}{bk\sin ak}\right.$$

$$\left.+\frac{2b^2}{W_pW_q\pi^3}\sum_{n=1}^{\infty}\frac{(\sin n\theta_1 - \sin n\theta_2)(\sin n\theta_3 - \sin n\theta_4)\cosh\dfrac{(a-x_p)\pi}{b}\sqrt{n^2-B^2}}{n^2\sqrt{n^2-B^2}\sinh\dfrac{a\pi}{b}\sqrt{n^2-B^2}}\right\}. \qquad (7.23)$$

The coupling impedance Z_{pq} is obtained in terms of closed form and single infinite series.

7.3.3 Self-coupling, or, probe feed input impedance

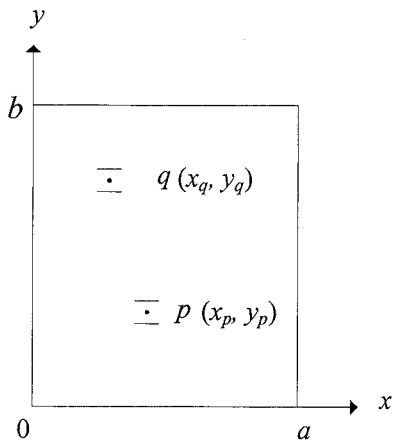


Figure 7.4: The locations of ports p and q where q approaching to port p.

Setting q=p in equation (7.16) gives

$$Z_{pp} = \frac{j\omega\mu h}{abW_p^2}\left\{-\frac{W_p^2}{k^2} + \frac{2a^2W_p^2}{\pi^2}\sum_{m=1}^{\infty}\frac{\cos^2\frac{m\pi}{a}x_p}{m^2-A^2} + \frac{2b^4}{\pi^4}\sum_{n=1}^{\infty}\frac{(\sin n\theta_1 - \sin n\theta_2)^2}{n^2(n^2-B^2)}\right.$$

$$\left. + \frac{4a^2b^2}{\pi^4}\sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\frac{\cos^2\frac{m\pi}{a}x_p(\sin n\theta_1 - \sin n\theta_2)^2}{n^2(m^2+D^2)}\right\} \tag{7.24}$$

$$Z_{pp} = \frac{j\omega\mu h}{abW_p^2}\left\{-\frac{W_p^2}{k^2} + \frac{2a^2W_p^2}{\pi^2}S_1(m) + \frac{2b^4}{\pi^4}S_2(n) + \frac{4a^2b^2}{\pi^4}S_3(m,n)\right\} \tag{7.25}$$

where, $S_1(m)$, $S_2(n)$ and $S_3(m, n)$ are given below. $S_1(m)$ is summed to a closed form

$$S_1(m) = \sum_{m=1}^{\infty}\frac{\cos^2\frac{m\pi}{a}x_p}{m^2-A^2} = \frac{1}{2}\sum_{m=1}^{\infty}\frac{1+\cos m\frac{2\pi}{a}x_p}{m^2-A^2}$$

$$= \frac{1}{2}\left[\frac{1}{2A^2} - \frac{\pi\cos A\pi}{2A\sin A\pi} + \frac{1}{2A^2} - \frac{\pi\cos A(\pi - 2\pi x_p/a)}{2A\sin A\pi}\right]$$

$$= \frac{1}{2}\left[\frac{1}{A^2} - \frac{\pi\left[\cos A\pi + \cos A\pi(1-2x_p/a)\right]}{2A\sin A\pi}\right]$$

$$= \frac{\pi^2}{2a^2k^2} - \frac{\pi^2[\cos ak + \cos k(a-2x_p)]}{4ak\sin ak}, \tag{7.26}$$

$$S_2(n) = \sum_{n=1}^{\infty}\frac{(\sin n\theta_1 - \sin n\theta_2)^2}{n^2(n^2-B^2)}, \tag{7.27}$$

and, in $S_3(m, n)$ the inner series is summed on the index m to a closed form to give the single infinite series.

$$S_3(m,n) = \sum_{n=1}^{\infty}\sum_{m=1}^{\infty}\frac{\cos^2\frac{m\pi}{a}x_p(\sin n\theta_1 - \sin n\theta_2)^2}{n^2(m^2+D^2)}$$

$$= \sum_{n=1}^{\infty}\frac{(\sin n\theta_1 - \sin n\theta_2)^2}{n^2}\cdot\frac{1}{2}\sum_{m=1}^{\infty}\frac{1+\cos m\frac{2\pi x_p}{a}}{m^2+D^2}$$

$$= \sum_{n=1}^{\infty}\frac{(\sin n\theta_1 - \sin n\theta_2)^2}{n^2}\cdot\frac{1}{2}\left[\frac{\pi\cosh D\pi}{2D\sinh D\pi} - \frac{1}{2D^2} + \frac{\pi\cosh D(\pi - 2\pi x_p/a)}{2D\sinh D\pi} - \frac{1}{2D^2}\right]$$

$$= \sum_{n=1}^{\infty} \frac{(\sin n\theta_1 - \sin n\theta_2)^2}{n^2} \left[\frac{\pi \left[\cosh D\pi + \cosh D\pi(1-2x_p/a) \right]}{4D \sinh D\pi} - \frac{1}{2D^2} \right]$$

$$= \frac{b\pi}{4a} \sum_{n=1}^{\infty} \frac{(\sin n\theta_1 - \sin n\theta_2)^2 \left[\cosh \frac{a\pi}{b}\sqrt{n^2 - B^2} + \cosh \frac{(a-2x_p)\pi}{b}\sqrt{n^2 - B^2} \right]}{n^2 \sqrt{n^2 - B^2} \sinh \frac{a\pi}{b}\sqrt{n^2 - B^2}} - \frac{b^2}{2a^2} S_2(n)$$

(7.28)

Substituting $S_1(m)$, and $S_3(m, n)$ from equations (7.26) and (7.28) respectively into equation (7.25) eliminates the terms $-W_p^2/k^2$, and the infinite series $S_2(n)$.

The new formula for Z_{pp} is then given by

$$Z_{pp} = j\omega\mu h \left\{ -\frac{\cos ak + \cos k(a-2x_p)}{2bk \sin ak} \right.$$

$$\left. + \frac{b^2}{W_p^2 \pi^3} \sum_{n=1}^{\infty} \frac{(\sin n\theta_1 - \sin n\theta_2)^2 \left[\cosh \frac{a\pi}{b}\sqrt{n^2 - B^2} + \cosh \frac{(a-2x_p)\pi}{b}\sqrt{n^2 - B^2} \right]}{n^2 \sqrt{n^2 - B^2} \sinh \frac{a\pi}{b}\sqrt{n^2 - B^2}} \right\}. \quad (7.29)$$

The self, or, input impedance Z_{pp} is obtained in terms of closed form and single infinite series.

To test the input impedance Z_{pp} formula, a 50 Ω matched rectangular patch with the dimensions of a=39.38 mm, b=47.42 mm was fabricated on a Duroid substrate with thickness h=0.79 mm as shown in Figure 7.5.

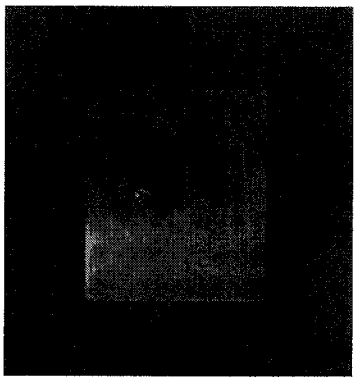
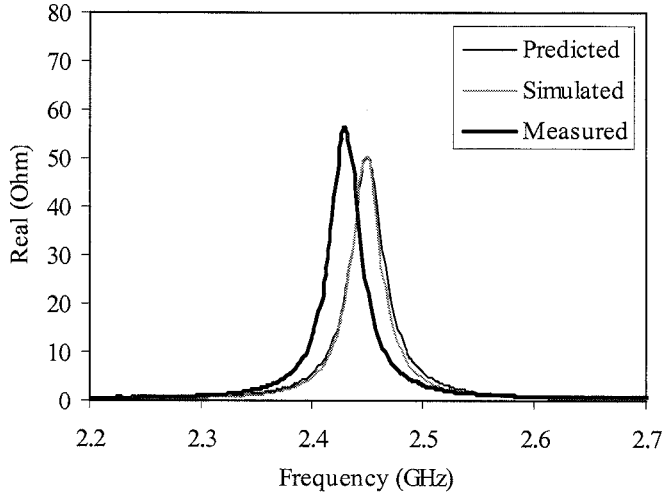


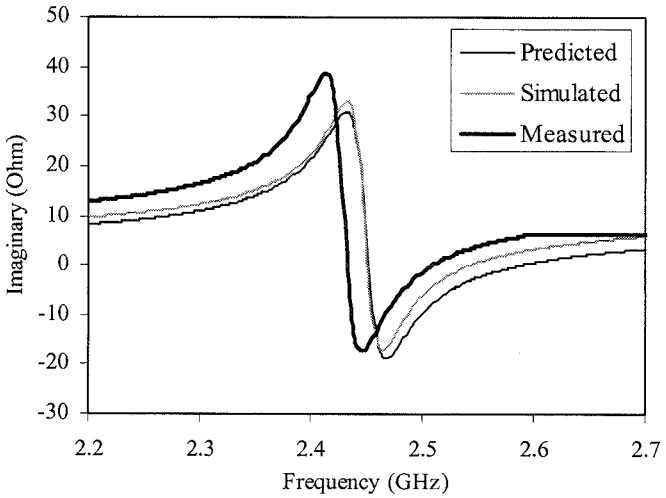
Figure 7.5: Fabricated probe feed rectangular patch.

The feed width, W_p is 1.26 mm, the simulated Q-factor is 68 and the probe feed location, is x_p=12.6 mm (0.32a), y_p=23.71 mm (0.5b).

The calculated, simulated and measured input impedance are compared and shown in Figures 7.6 (a) and (b).



(a)



(b)

Figure 7.6: Predicted, simulated and measured Z_{in}. (a) Real part. (b) Imaginary part.

Good agreement is obtained between the predicted, simulated and measured results for the input impedance. The predicted, simulated and measured input impedances are 49.3+j0.4 Ω at 2.452 GHz (0.1% shift from 2.45 GHz), 50.4+j4 Ω at 2.45 GHz and

$55.3+j2.3\ \Omega$ at 2.432 GHz (0.7% shift from 2.45 GHz). For the calculation an upper limit of 10 was used in evaluating the infinite series.

7.4 Summary

For the coupling impedance between a probe feed and a perimeter port on a rectangular segment a new explicit computationally efficient coupling impedance formula has been derived. A new explicit formula for the self, or, input impedance has also been derived. To test the input impedance formula a $50\ \Omega$ matched rectangular patch has been fabricated. The predicted and simulated results for the antenna show good agreement with the measured results. The above formulas are used in the following chapter in the evaluation of the input impedance of an H-shaped patch antenna.

CHAPTER 8 AN APPROACH TO THE DESIGN OF AN H-SHAPED MICROSTRIP PATCH ANTENNA

8.1 Introduction

Modern communication systems require a compact, lightweight and low-cost transmitter front-end. The H-shaped microstrip patch antenna has advantages in that it is compact [98], [129] and can also be used in multi-band application [130], [131] as it can generate four mode frequencies, f_1, f_2, f_3, and, f_4. This antenna can also be used as a load in an AIA design [132], [133].

In [98] it is shown that the H-shaped patch antenna is more compact than the rectangular patch antenna. The effect of the dimensions of an H-shaped antenna on the first mode frequency, f_1, and, radiation patterns was studied in [129]. The H-shaped antenna with a probe feed was proposed for dual-frequency operation in [130]. Parametric studies were performed to study the effects of the antenna dimensions on mode frequencies, f_1 and f_3, the frequency ratio between two mode frequencies, and the radiation patterns. A probe feed H-shaped patch antenna was designed for dual-, triple-, and, quad-frequency operations in [131]. Using the electric and magnetic walls along the antenna lines of symmetry formulas for the first three mode frequencies were derived. A formula for the fourth mode was also derived by modelling the patch as a step impedance resonator. The probe feed location was also discussed in relation to the number of operational frequency bands available. In [132], it was demonstrated that a microstrip feed H-shaped patch antenna was suitable for AIA design, where, the antenna radiates at the fundamental mode frequency while suppressing the PA's second and third harmonics. In [133] a microstrip feed H-shaped patch antenna was used to realise an oscillator-type AIA to suppress the harmonic radiation. A new approach to the design of compact high efficiency AIA using a probe feed H-shaped patch antenna is discussed in Chapter 9. The above papers [98],

[129]-[133] do not present any clear description on how to determine the design parameters of the antenna.

In this chapter an approach to obtain a feasible set of the design parameters is presented [134]. The four geometric design parameters L_1, L_2, W_1, W_2, and, the location of the probe feed are shown in Figure 8.1.

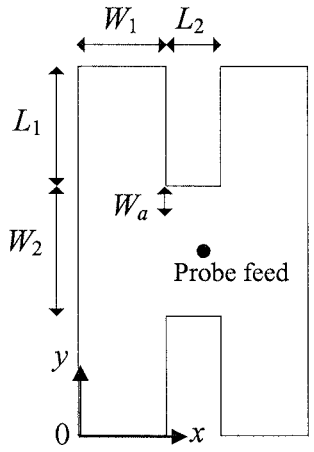


Figure 8.1: H-shaped microstrip patch antenna geometry.

In Figure 8.1 the fifth design parameter W_a is the distance from the upper edge of the horizontal segment to the line of maximum current density at a given mode frequency.

A basic requirement is for the antenna to radiate at a pre-assigned operational frequency. The design requirements do not define uniquely the design parameters, therefore, values of some parameters must be assigned in the design calculations. In this chapter the following aspects of a design approach are discussed in detail.

Using odd and even mode analysis, formulas for all the four mode frequencies in terms of the five design parameters, are derived in Section 8.2.

Relationships between the parameter pairs W_1, W_2, and, W_a, W_2 are deduced from current density studies as discussed in Section 8.3. For the higher mode frequencies, f_2, f_3, f_4, it was found that $W_a=W_2/4$. However, for the first mode frequency, f_1, it was found that W_a depends on the ratio, W_2/W_1. Based on the studies of the current density maps, the

values of W_a for three ratios W_2/W_1=1, 1.5, 2 was estimated. Using these values of W_a it was found that a good agreement was obtained between the predicted and simulated values at all four mode frequencies. Further, it is shown in this section that by assuming a value for W_1 the five unknown design parameters in the formula for the first mode, f_1 are now reduced to two, L_1 and L_2.

In Section 8.4 it is shown how, by using a two dimensional plot, feasible values of L_1, L_2, can be determined. Six antennas were designed and the results obtained were all in good agreement with the results obtained from simulation. Two of these antennas were fabricated and the measured results were also in good agreement with the predicted and simulated results.

For impedance matching, it is necessary to establish the location of the probe feed, and, to calculate the input impedance of the antenna at the pre-assigned operational frequency. To compute the input impedance of this antenna the segmentation method [135], [136] was used and is discussed in Section 8.5. A new explicit matrix formula for the probe feed input impedance [125] is obtained which uses a new technique to reduce the number of coplanar matrix circuit equations and this is presented in detail in Section 8.6. From an inspection of the current density distribution, it is shown that the horizontal segment gave the low impedance. In Section 8.7 the application of the input impedance formula to obtain the feed location for a 50 Ω match is presented. The antenna was then fabricated and the predicted, simulated, and, measured values of input impedance at the pre-assigned frequency of 2.45 GHz showed good agreement. Based on this work two papers have been published in [125] and [134].

8.2 Determination of the Resonant Mode Frequencies Based on Odd and Even Mode Analysis

The H-shaped antenna structure has four-fold symmetry and hence can generate four resonant mode frequencies. It is possible to obtain the relationship between the five design parameters and the four mode frequencies by applying odd and even mode conditions, as shown in Figure 8.2.

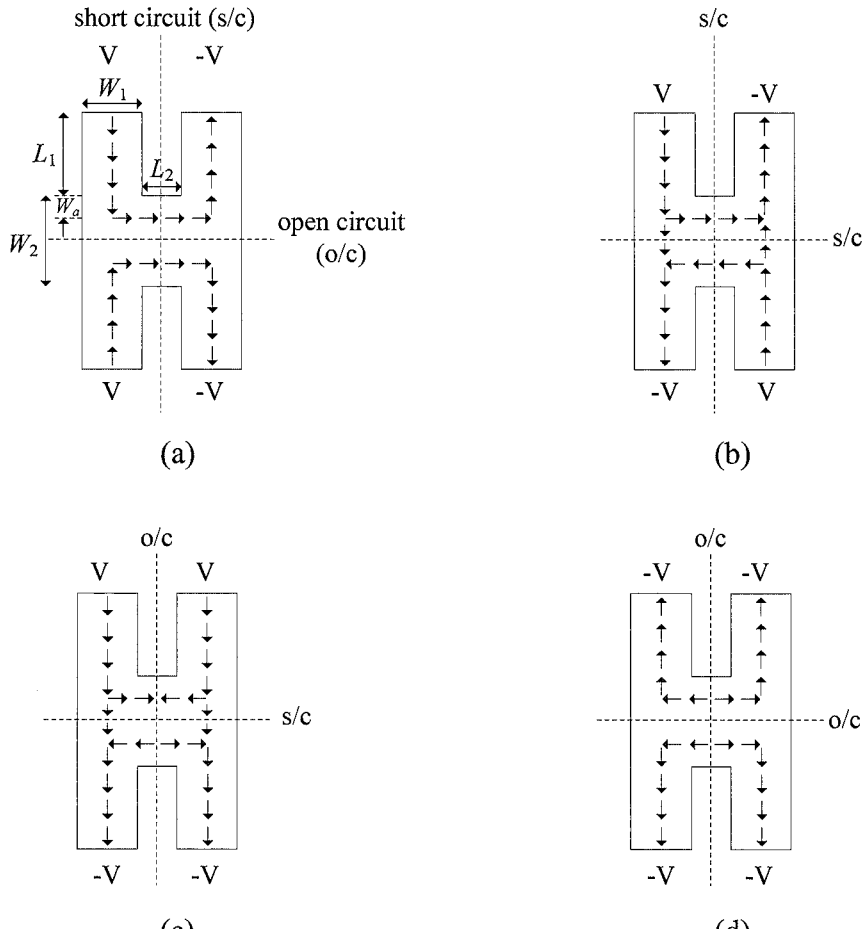


Figure 8.2: Current path. (a) f_1. (b) f_2. (c) f_3. (d) f_4.

In Figure 8.2, the arrows show the paths of the maximum current density which are used to determine the formulas for the four mode frequencies. As the antenna has symmetric four-fold symmetry geometry, the formulas for the four mode frequencies can be obtained by determining the current path length in one-quarter of the antenna geometry, as shown below.

Figure 8.3 shows the equivalent microstrip line circuit for the first mode, f_1 (corresponding to Figure 8.2(a)), where the microstrip line of width W_1, and, length L_1+W_a, is connected in series with a microstrip line of width $W_2/2$, and, length $W_1/2+L_2/2$.

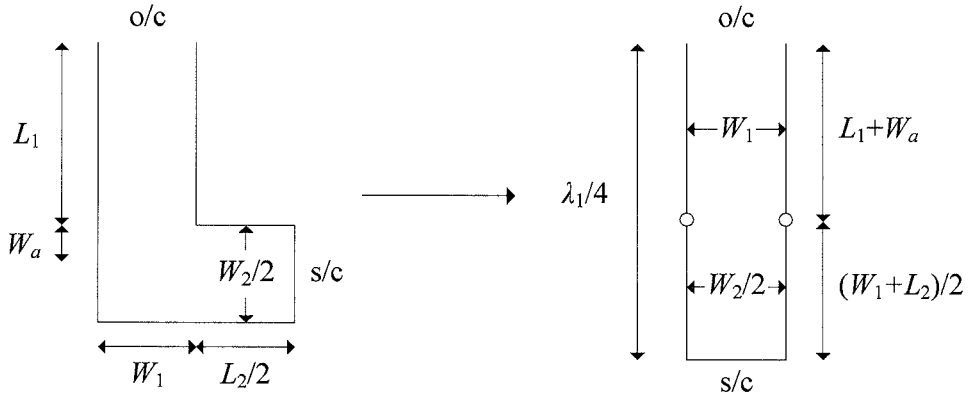


Figure 8.3: Equivalent microstrip line circuit for mode f_1.

For this mode frequency, $L_1 + W_a + W_1/2 + L_2/2 = \lambda_1/4$, then, f_1 is given by

$$f_1 = \frac{c_0}{4(L_1 + W_a)\sqrt{\varepsilon_{reff1}} + 2(W_1 + L_2)\sqrt{\varepsilon_{reff2}}} \tag{8.1}$$

where,

$$\varepsilon_{reff1} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\frac{1}{\sqrt{1 + \frac{12h}{W_1}}} \tag{8.2}$$

and,

$$\varepsilon_{reff2} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\frac{1}{\sqrt{1 + \frac{24h}{W_2}}}. \tag{8.3}$$

Figure 8.4 shows the equivalent microstrip line circuit for the second mode, f_2 (corresponding to Figure 8.2(b)), where the microstrip line of width W_1, and, length $L_1+W_2/4$, is connected in series with an effective microstrip line of width W_1, and, length L_a.

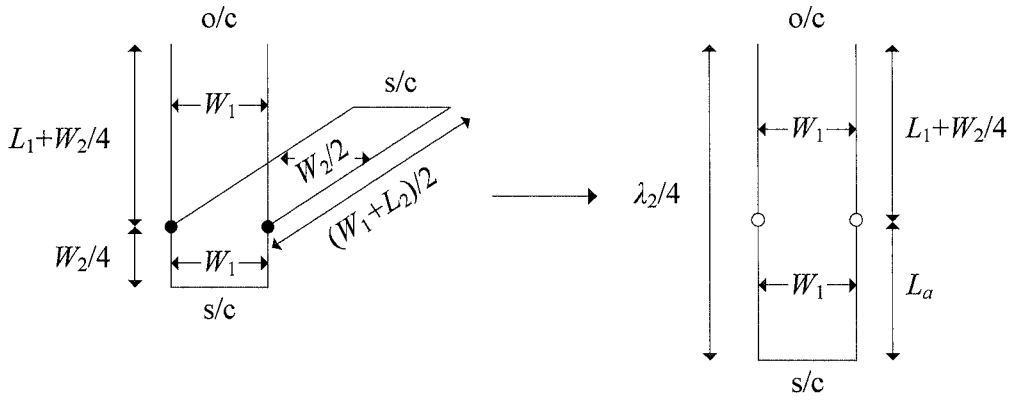


Figure 8.4: Equivalent microstrip line circuit for mode f_2.

For this mode frequency, $L_1 + W_2/4 + L_a = \lambda_2/4$, then, f_2 is given by

$$f_2 = \frac{c_0}{(4L_1 + W_2 + 4L_a)\sqrt{\varepsilon_{reff1}}}, \tag{8.4}$$

where, L_a, the effective length, takes into account two parallel short circuit microstrip lines of length $(W_1+L_2)/2$, and, width $W_2/2$, and, of length $W_2/4$, and, width W_1, so that

$$L_a = \frac{1}{2}\frac{Z_2 W_2 (W_1 + L_2)}{Z_1 W_2 \sqrt{\frac{\varepsilon_{reff1}}{\varepsilon_{reff2}}} + 2Z_2(W_1 + L_2)}, \tag{8.5}$$

where, the characteristic impedance of the two microstrip lines of widths W_1, $W_2/2$, are given by equations (8.6) and (8.7).

$$Z_1 = \frac{120\pi}{\sqrt{\varepsilon_{reff1}}\left(\frac{W_1}{h} + 1.393 + 0.667\ln\left(\frac{W_1}{h} + 1.444\right)\right)} \tag{8.6}$$

$$Z_2 = \frac{120\pi}{\sqrt{\varepsilon_{reff2}}\left(\frac{W_2}{2h} + 1.393 + 0.667\ln\left(\frac{W_2}{2h} + 1.444\right)\right)}. \tag{8.7}$$

Figure 8.5 shows the equivalent microstrip line circuit for the third mode, f_3 (corresponding to Figure 8.2(c)), where the microstrip line of width W_1, and, length L_1, is connected in series with an effective microstrip line of width W_1, and, length L_b.

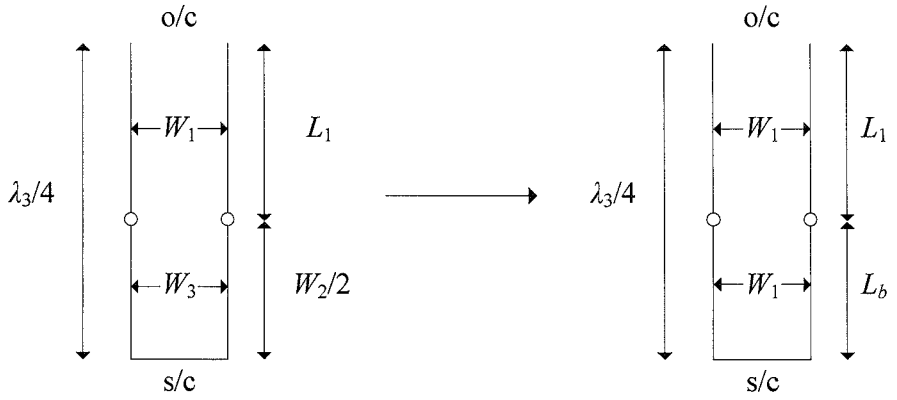


Figure 8.5: Equivalent microstrip line circuit for mode f_3.

For this mode frequency, $L_1 + L_b = \lambda_3 / 4$, then, f_3 is given by

$$f_3 = \frac{c_0}{(4L_1 + 4L_b)\sqrt{\varepsilon_{reff1}}}, \tag{8.8}$$

where, L_b, the effective length, takes into account the effect of the short circuit microstrip line of length $W_2/2$, and, width W_3, so that

$$L_b = \frac{Z_3}{Z_1}\frac{W_2}{2}\sqrt{\frac{\varepsilon_{reff3}}{\varepsilon_{reff1}}}, \tag{8.9}$$

where,

$$\varepsilon_{reff3} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\frac{1}{\sqrt{1 + \frac{12h}{W_3}}}, \tag{8.10}$$

where, the characteristic impedance of the microstrip line of width W_3 is given by equation (8.11).

$$Z_3 = \frac{120\pi}{\sqrt{\varepsilon_{reff3}}\left(\frac{W_3}{h} + 1.393 + 0.667\ln\left(\frac{W_3}{h} + 1.444\right)\right)}, \tag{8.11}$$

and, where,

$$W_3 = W_1 + \frac{L_2}{2}. \tag{8.12}$$

The equations for f_2 and f_3 are as derived in [131], but presented in a more practical way using microstrip line form.

Figure 8.6 shows the equivalent microstrip line circuit for the fourth mode, f_4 (corresponding to Figure 8.2(d)), where the microstrip line of width W_1 and length L_1, is connected in series with an effective microstrip line of width W_1 and length L_c.

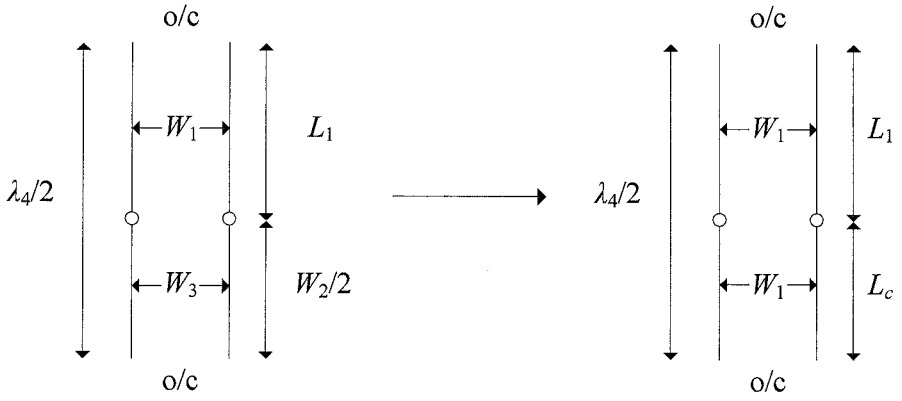


Figure 8.6: Equivalent microstrip line circuit for mode f_4.

For this mode frequency, $L_1 + L_c = \lambda_4 / 2$, so that, f_4 is given by

$$f_4 = \frac{c_0}{(2L_1 + 2L_c)\sqrt{\varepsilon_{reff1}}}, \tag{8.13}$$

where, L_c, the effective length, takes into account the effect of the open circuit microstrip line of length $W_2/2$ and width W_3, so that

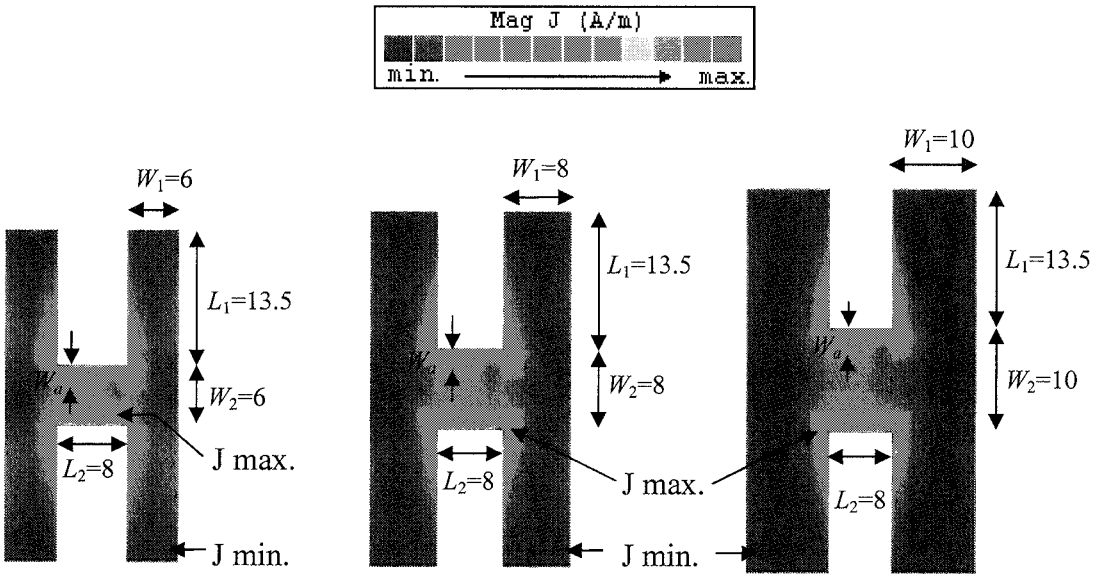
$$L_c = \frac{Z_1}{Z_3}\frac{W_2}{2}\sqrt{\frac{\varepsilon_{reff3}}{\varepsilon_{reff1}}}. \tag{8.14}$$

This is a new and a very simple formula for the fourth mode frequency, f_4 [134]. The details of the derivation of the formulas for f_1, f_2, f_3 and f_4 are given in *Appendix 8A*.

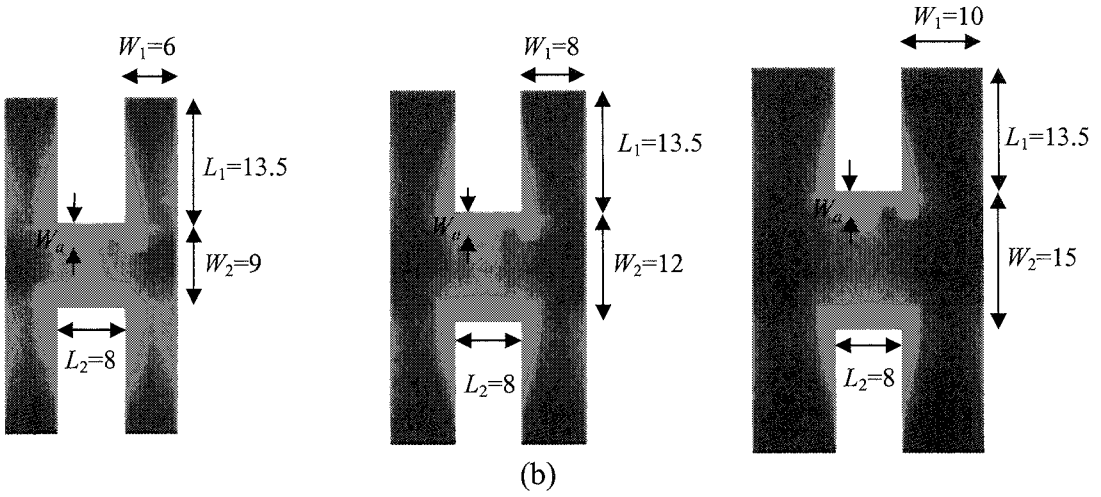
8.3 Application of Empirical Parametric Studies to Obtain Relationships Between Design Parameters

In equation (8.1) for the fundamental mode frequency, f_1, there are five design parameters L_1, L_2, W_1, W_2 and W_a, so, there is no unique set of parameter values that will satisfy a given value of f_1. Sheta [131] assumed that, in this formula the value of W_a is $W_2/4$. However, from preliminary studies it was found that W_a is a function of the ratio W_2/W_1. Hence extensive empirical parametric studies were performed in order to establish relationships between W_a and W_2/W_1. For this purpose, the current density maps for eighteen antenna geometries were studied, which resulted in a reduction to three design parameters in the formula for f_1.

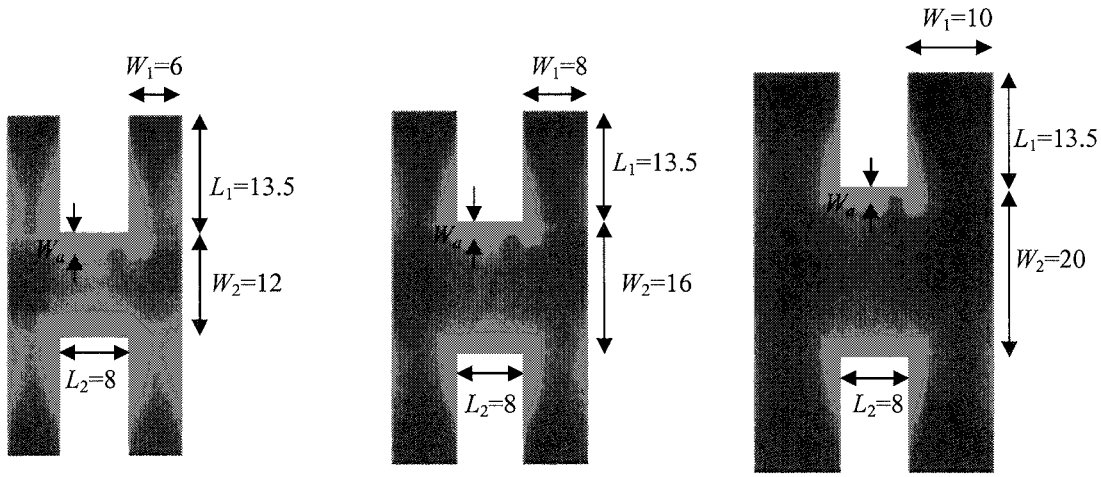
The initial antenna structure studied used L_1=13.5 mm, L_2=8 mm, and, a substrate, thickness of h=1.57 mm, with ε_r=2.2, which are the values employed in [131]. Using ADS software tool, studies for each of the three ratios, W_2/W_1=1, 1.5, and, 2 were carried out. In each case W_1 was assigned the values, W_1=2 mm, 4 mm, 6 mm, 8 mm, 10 mm, and, 12 mm, giving altogether eighteen case studies. Nine of the current density maps are shown in Figure 8.7.



(a)



(b)

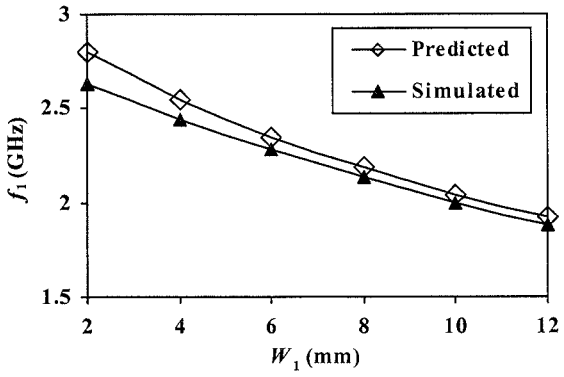


(c)

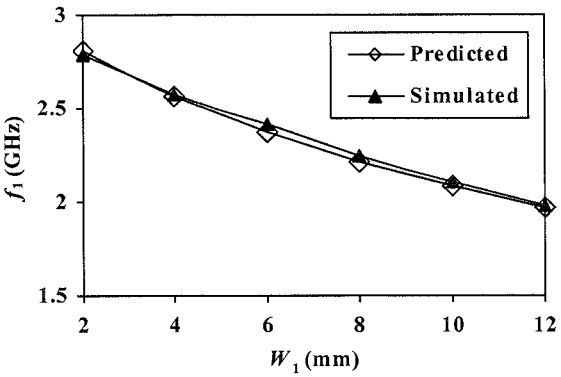
Figure 8.7: Simulated f_1's current density distributions. (a) W_2/W_1=1. (b) W_2/W_1=1.5. (c) W_2/W_1=2.

Based on the maximum current density distribution across the width, W_2, in the horizontal part of the antenna (see Figure 8.7), the results showed that for each of the three ratios, W_2/W_1=1, 1.5, 2, the approximate average values of W_a, were, $W_a \approx W_2/4$, $W_a \approx W_2/8$, and, $W_a \approx W_2/12$.

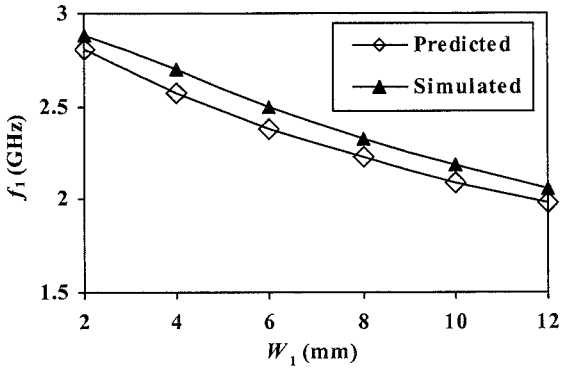
For the first mode frequency, f_1, the above relationships for W_a was used and the values of W_1 were varied from 2-12 mm in steps of 2 mm, for each of the ratios W_2/W_1=1, 1.5, 2, as shown in Figure 8.8. As can be seen in Figure 8.8 there is a good agreement between the predicted and simulated values for the first mode frequency, f_1 with varying from 1.9-2.8 GHz.



(a)



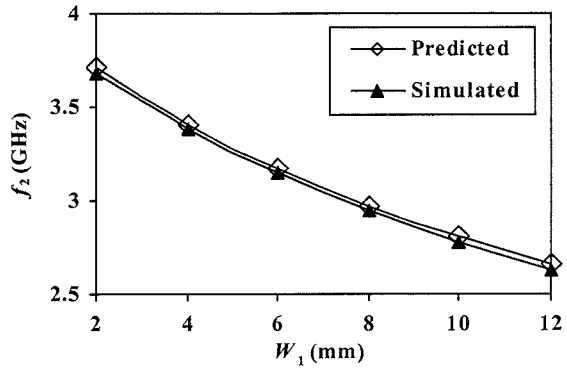
(b)



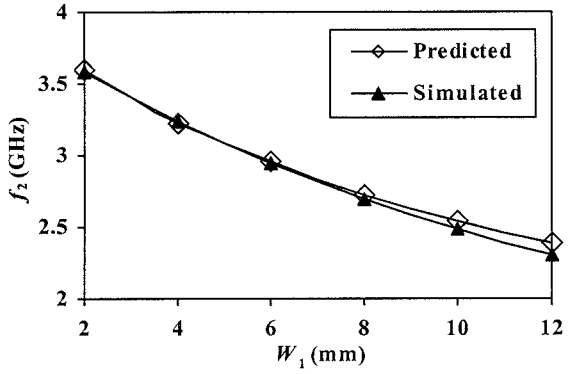
(c)

Figure 8.8: Predicted and simulated f_1. (a) W_2/W_1=1. (b) W_2/W_1=1.5. (c) W_2/W_1=2.

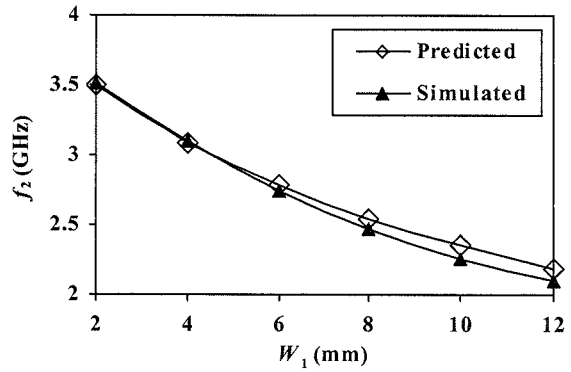
Also for each ratio W_2/W_1=1, 1.5, 2, graphical verification of the equations (8.4), (8.8), and, (8.13) for f_2, f_3, f_4 is shown in Figures 8.9, 8.10, and, 8.11. Good agreements are obtained between the predicted and simulated results.



(a)

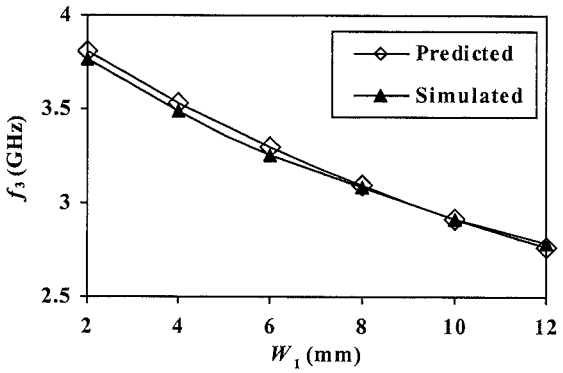


(b)

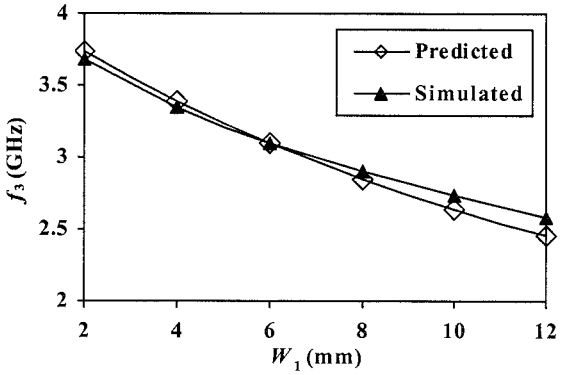


(c)

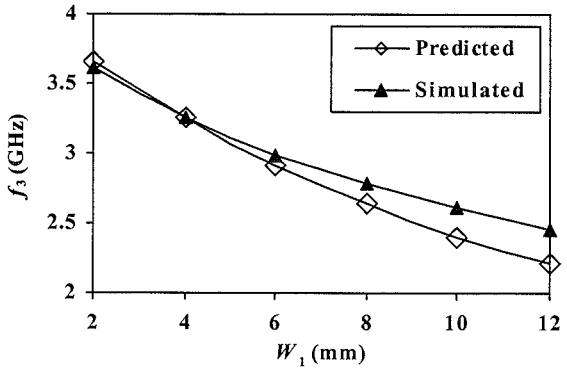
Figure 8.9: Predicted and simulated f_2. (a) W_2/W_1=1. (b) W_2/W_1=1.5. (c) W_2/W_1=2.



(a)



(b)



(c)

Figure 8.10: Predicted and simulated f_3. (a) W_2/W_1=1. (b) W_2/W_1=1.5. (c) W_2/W_1=2.

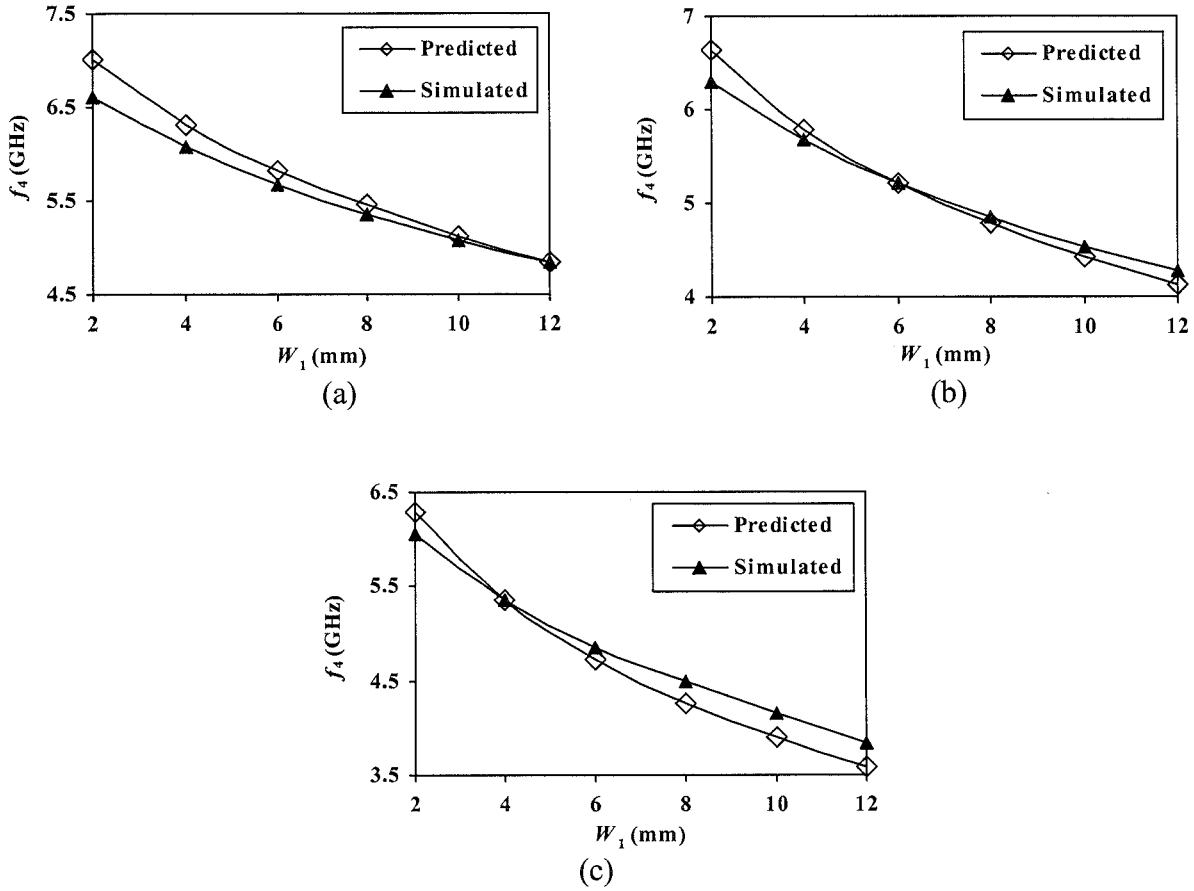


Figure 8.11: Predicted and simulated f_4. (a) W_2/W_1=1. (b) W_2/W_1=1.5. (c) W_2/W_1=2.

These studies have shown that, for a given value, r^*, of the ratio, W_2/W_1, then, W_a has the value W_2/c^*, where c^* is fixed from the studies. That is, the parameters W_2 and W_a can be expressed as $W_2 = r^* W_1$, and, $W_a = W_2/c^* = (r^*/c^*)W_1$. Thus the parameter set L_1, L_2, W_1, W_2, and, W_a can effectively be replaced by the set, L_1, L_2, W_1, $r^* W_1$, $(r^*/c^*)W_1$. At this stage the number of unknown parameters has been reduced from five to three.

8.4 An Approach to the Design of an H-shaped Microstrip Patch Antenna

The design approach for an H-shaped antenna to operate at the fundamental mode frequency is described as below.

1. Select a numerical value r^* for the ratio W_2/W_1 in the range 1-2.
2. Select a practical value W_1^* for W_1 between 6-12 mm.

   (Steps 1 and 2 then fix the numerical values for W_1^*, and, W_2^*.)

3. Construct the current density distribution maps to obtain the value of $W_a=W_a^*$, in terms of W_2, where $W_a^*=W_2^*/c^*$.

4. Select the numerical value of the antenna operating frequency, f_1^*.

5. Construct the function, $F(L_1, L_2)$, where,

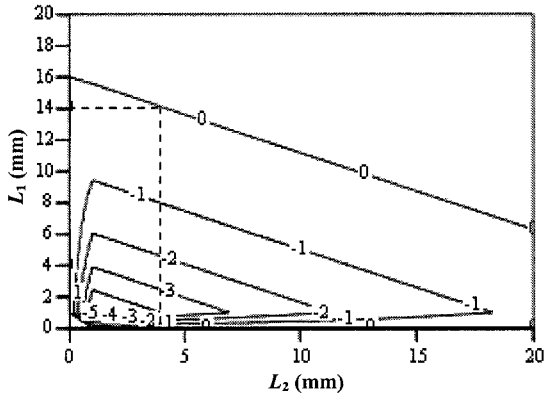
$$F(L_1, L_2) = f_1^* - f_1(L_1, L_2: W_1^*, W_2^*, W_a^*). \quad (8.15)$$

6. Obtain a contour plot of $F(L_1, L_2)$ to determine the zero contour line of $F(L_1, L_2)$.

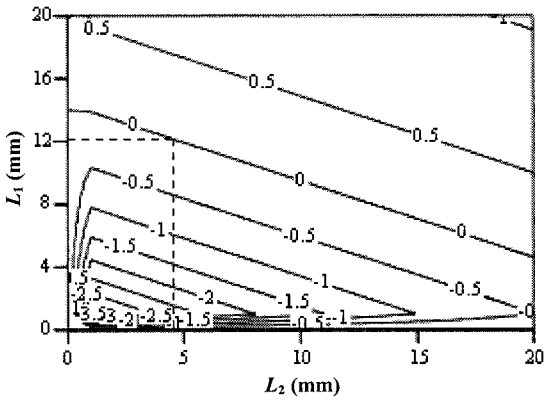
7. Select any practical pair of values L_1, L_2 on the zero contour line to complete the geometric design of the antenna structure.

The above procedure has been applied to design six antennas, each operating at f_1^*=2.45 GHz. A Duroid substrate with a thickness of 0.79 mm was used. Three antennas (*A*, *B*, *C*) were designed using W_2/W_1=1, with W_1=6 mm, 8 mm, and, 10 mm and three antennas (*D*, *E*, *F*) were designed using W_2/W_1=1.5, with W_1=6 mm, 8 mm, and, 10 mm.

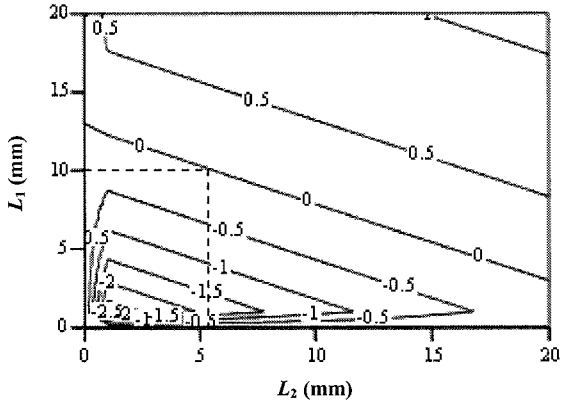
The six two dimensional contour plots of $F(L_1, L_2)$ are shown in Figures 8.12 and 8.13, where, all points on the zero contours represent a feasible solution consistent with the pre-assigned operational frequency.



(a)

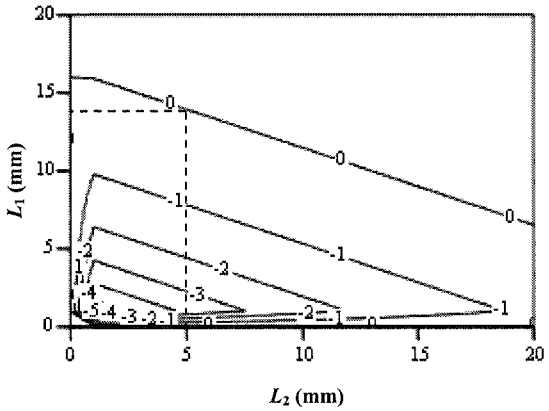


(b)

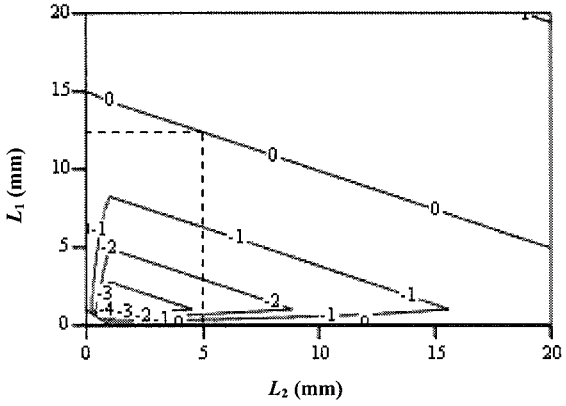


(c)

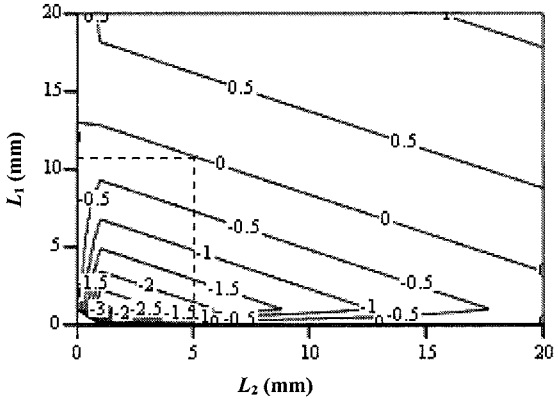
Figure 8.12: Two dimensional contour plot for antenna with W_2/W_1=1. (a) W_1=6 mm. (b) W_1=8 mm. (c) W_1=10 mm.



(a)



(b)



(c)

Figure 8.13: Two dimensional contour plot for antenna with W_2/W_1=1.5. (a) W_1=6 mm. (b) W_1=8 mm. (c) W_1=10 mm.

The contour lines labelled -1, -0.5, 0.5, 1 indicate that the f_1 (L_1, L_2) = 3.45 GHz, 2.95 GHz, 1.95 GHz, and, 1.45 GHz, respectively. Also for the f_1 (L_1, L_2) < 0, the narrow gaps between the contours show that the sensitivity of L_1, L_2 increases with frequency.

The design parameters for the six antennas, *A*, *B*, *C*, *D*, *E*, and, *F* operating at 2.45 GHz for ratios W_2/W_1=1, 1.5 are listed in Tables 8.1 and 8.2.

Antenna	W_2/W_1	W_1 (mm)	W_2 (mm)	L_1 (mm)	L_2 (mm)
A	1	6	6	14	4.2
B	1	8	8	12	4.8
C	1	10	10	10	5.5

Table 8.1: Dimensions for antennas *A*, *B* and *C* where W_2/W_1=1.

Antenna	W_2/W_1	W_1 (mm)	W_2 (mm)	L_1 (mm)	L_2 (mm)
D	1.5	6	9	13.9	5
E	1.5	8	12	12.3	5
F	1.5	10	15	10.8	5

Table 8.2: Dimensions for antennas *D*, *E* and *F* where W_2/W_1=1.5.

These design parameters in Tables 8.1 and 8.2 were then used and the antennas were modelled to obtain the corresponding values of the four frequencies f_1, f_2, f_3, and, f_4. A probe feed location (x, y), located on the horizontal segment, was chosen to ensure that all the four mode frequencies, f_1, f_2, f_3, f_4 were able to be generated.

The predicted and simulated results for all six antennas are compared in Tables 8.3, 8.4, 8.5, 8.6, 8.7 and 8.8. Good agreement between the predicted and simulated values of the mode frequency has been obtained.

Mode frequency (GHz)	Predicted (GHz)	Simulated (GHz)	Error (%)
f_1	2.45	2.40	2
f_2	3.01	2.98	1
f_3	3.08	3.09	0.3
f_4	5.67	5.64	0.5

Table 8.3: Predicted and simulated mode frequencies (f_1, f_2, f_3 and f_4) for antenna *A*.

Mode frequency (GHz)	Predicted (GHz)	Simulated (GHz)	Error (%)
f_1	2.45	2.37	3.3
f_2	3.18	3.15	0.9
f_3	3.27	3.29	0.6
f_4	5.89	5.88	0.2

Table 8.4: Predicted and simulated mode frequencies (f_1, f_2, f_3 and f_4) for antenna *B*.

Mode frequency (GHz)	Predicted (GHz)	Simulated (GHz)	Error (%)
f_1	2.45	2.35	4.1
f_2	3.38	3.35	0.9
f_3	3.51	3.53	0.6
f_4	6.14	6.17	0.5

Table 8.5: Predicted and simulated mode frequencies (f_1, f_2, f_3 and f_4) for antenna *C*.

Mode frequency (GHz)	Predicted (GHz)	Simulated (GHz)	Error (%)
f_1	2.45	2.48	1.2
f_2	2.83	2.8	1
f_3	2.91	2.96	1.7
f_4	5.1	5.15	1

Table 8.6: Predicted and simulated mode frequencies (f_1, f_2, f_3 and f_4) for antenna *D*.

Mode frequency (GHz)	Predicted (GHz)	Simulated (GHz)	Error (%)
f_1	2.45	2.46	0.4
f_2	2.86	2.79	2.4
f_3	2.92	3.03	3.8
f_4	5.06	5.16	2

Table 8.7: Predicted and simulated mode frequencies (f_1, f_2, f_3 and f_4) for antenna *E*.

Mode frequency (GHz)	Predicted (GHz)	Simulated (GHz)	Error (%)
f_1	2.45	2.44	0.4
f_2	2.88	2.77	3.8
f_3	2.92	3.1	6.1
f_4	5.01	5.19	3.6

Table 8.8: Predicted and simulated mode frequencies (f_1, f_2, f_3 and f_4) for antenna *F*.

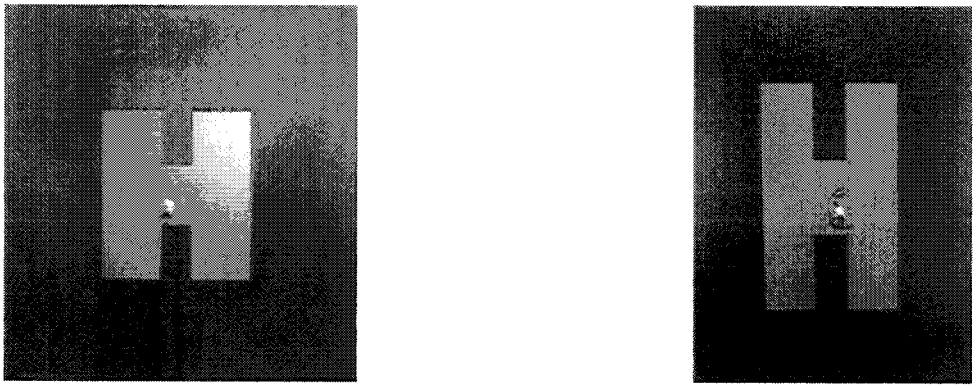
From the six antennas, antenna *C* with a ratio W_2/W_1=1, and, antenna *E* with a ratio W_2/W_1=1.5 were chosen, and, L_1, L_2 of each antenna was fine tuned to radiate at 2.45 GHz.

For comparison, the final design parameters (L_1, L_2, W_1, W_2) and probe feed locations, (x, y), for the two antennas are given in Table 8.9.

Antenna	W_2/W_1	W_1 (mm)	W_2 (mm)	L_1 (mm)	L_2 (mm)	x, y (mm)
C	1	10	10	9.35	5.2	11.2, 11.4
E	1.5	8	12	12.35	5.2	12.2, 15

Table 8.9: Dimensions and probe feed locations, (x, y), for antennas C and E.

To compare the predicted and simulated results, the antennas, C and E were fabricated and tested. The fabricated antennas are shown in Figures 8.14(a) and (b).



(a) (b)

Figure 8.14: Fabricated H-shaped antennas. (a) Antenna C. (b) Antenna E.

The predicted, simulated and measured mode frequencies, f_1, f_2, f_3 and f_4 are shown in Tables 8.10 and 8.11, showing the percentage error is the difference between predicted and measured mode frequencies.

Mode frequency (GHz)	Predicted (GHz)	Simulated (GHz)	Measured (GHz)	Error (%)
f_1	2.55	2.45	2.43	4.7
f_2	3.54	3.49	3.44	2.8
f_3	3.66	3.70	3.67	0.3
f_4	6.41	6.45	6.38	0.5

Table 8.10: Predicted, simulated and measured mode frequencies (f_1, f_2, f_3 and f_4) for antenna C.

Mode frequency (GHz)	Predicted (GHz)	Simulated (GHz)	Measured (GHz)	Error (%)
f_1	2.44	2.45	2.43	0.4
f_2	2.85	2.79	2.76	3.2
f_3	2.92	3.03	3.01	3.1
f_4	5.03	5.13	5.09	1.2

Table 8.11: Predicted, simulated and measured mode frequencies (f_1, f_2, f_3 and f_4) for antenna *E*.

The results show that there is a good agreement between the predicted, simulated and measured values for these modes with a maximum error of 4.7%. For the first mode frequency, f_1 it can be seen that excellent accuracy is obtained for the Antenna *E* with the ratio W_2/W_1=1.5.

For matching the antenna input impedance to 50 Ω, it is necessary to establish the location of the probe feed, and, to calculate the input impedance of the antenna at the pre-assigned operational frequency. In the next section, a new explicit matrix input impedance formula, is derived, and, used to establish the probe feed location to obtain a close match to 50 Ω at 2.45 GHz for antenna *E*.

8.5 The Segmentation Method

When the Green's function for an antenna geometry is not available the segmentation method can be used if the geometry can be "segmented" into 'segments' each with a known Green's function. The segmentation method was first proposed by Okoshi and Takeuchi [136]. An application of matrix circuit analysis to the combined structure gives the input impedance. At first, the segmentation method was formulated in terms of S-matrices [136], and later replaced by Z-matrices [135], which are more efficient in computation time.

The basis of the method is that current density distribution on the patch is conserved on each component segment of the segmented structure. For example an antenna geometry

of the form as shown in Figure 8.15 can be "segmented" into the two segments α, β. The segments are connected electrically by interconnecting ports as shown in Figure 8.16. The function of these ports is to maintain the original current sheet on each segment of the antenna as shown in Figure 8.15.

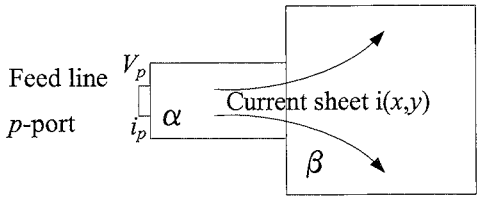


Figure 8.15: Composite structure.

A connecting port structure is shown in Figure 8.16.

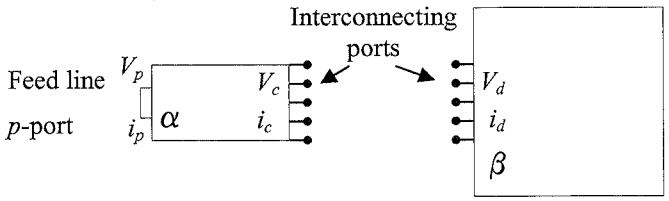


Figure 8.16: Segment structure.

The electrical equivalence of the original and segmental structure is shown in Figure 8.17.

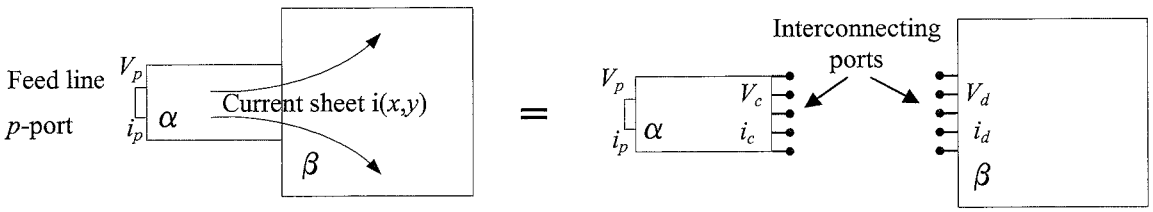


Figure 8.17: Current sheet on antenna.

In the analysis the ports are assigned electric currents and voltages which emulate approximately the original currents and voltages in the composite structure. The electric circuit equations connecting the voltages and currents at the connecting ports are used to determine the antenna input impedance, as illustrated below.

For a two segments structure (see Figure 8.18) there are three matrix circuit equations.

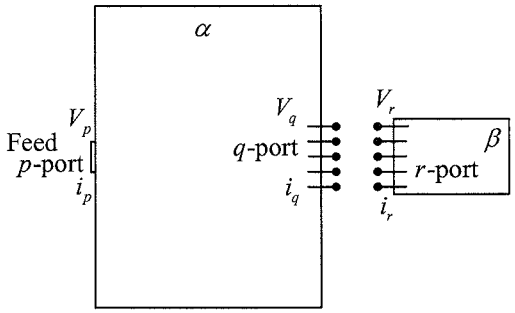


Figure 8.18: Interport structure for two segments.

For the α-segment

$$V_p = Z_{pp} i_p + Z_{pq} i_q \tag{8.16}$$

and,

$$V_q = Z_{qp} i_p + Z_{qq} i_q . \tag{8.17}$$

For the β-segment,

$$V_r = Z_{rr} i_r . \tag{8.18}$$

Since $V_q = V_r$, and, $i_q = -i_r$, therefore from equations (8.17) and (8.18),

$$Z_{qp} i_p + Z_{qq} i_q = -Z_{rr} i_q$$

so that, $(Z_{qq} + Z_{rr}) i_q = -Z_{qp} i_p$

hence, $i_q = -(Z_{qq} + Z_{rr})^{-1} Z_{qp} i_p .$ (8.19)

Substituting i_q from equation (8.19) into equation (8.16) gives

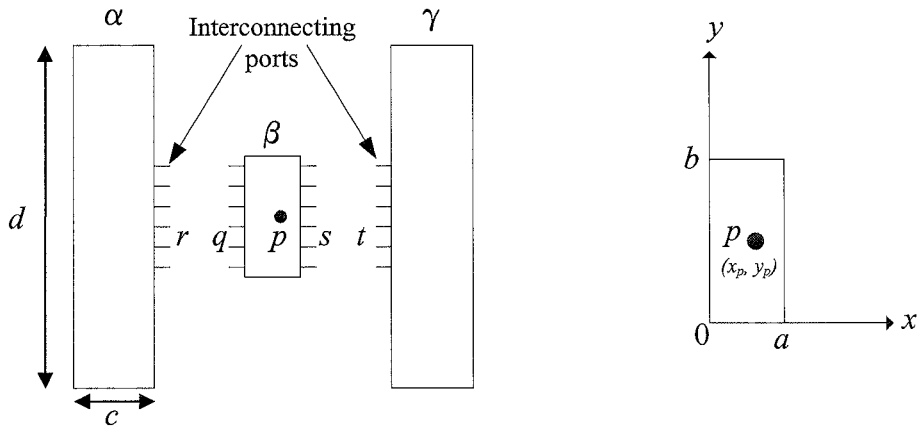
$$V_p = Z_{pp} i_p + Z_{pq}(-1)(Z_{qq} + Z_{rr})^{-1} Z_{qp} i_p$$

so that the matrix input impedance formula for, Z_{in}, is given by

$$Z_{in} = \frac{V_p}{i_p} = Z_{pp} - Z_{pq}(Z_{qq} + Z_{rr})^{-1} Z_{qp} . \tag{8.20}$$

8.6 Derivation of the Matrix Input Impedance Formula

The segmentation structure of the antenna, with connecting ports q, r, s, t, is shown below in Figure 8.19(a).



(a) (b)

Figure 8.19: H-shaped microstrip patch antenna (a) Segmental structure (b) β-segment.

In the conventional analysis based on the coplanar circuit analysis [121] there are five voltage/current circuit equations, one each for V_p, V_q, V_r, V_s, and, V_t. These five equations can be reduced to an equivalent set of three equations using a new technique [125] in which the two equations for the α and γ segments are imbedded into a single equivalent matrix equation. This effectively combines the two segments α, γ into a single quasi-segment. Also the equations for V_q and V_s can likewise be combined into a single equivalent matrix equation. That is four of the conventional equations are replaced by two

equivalent equations leaving a system of three equations to be solved for the input impedance, $Z_p=V_p/i_p$. This technique is applied as follow.

The five conventional circuit equations are

$$V_p = Z_{pp}i_p + Z_{pq}i_q + Z_{ps}i_s \tag{8.21}$$

$$V_q = Z_{qq}i_q + Z_{qs}i_s + Z_{qp}i_p \tag{8.22}$$

$$V_s = Z_{ss}i_s + Z_{sq}i_q + Z_{sp}i_p \qquad (Z_{ss} = Z_{qq}), (Z_{sq} = Z_{qs}) \tag{8.23}$$

$$V_r(=V_q) = Z_{rr}i_r \qquad (i_r = -i_q) \tag{8.24}$$

$$V_t(=V_s) = Z_{tt}i_t \qquad (i_t = -i_s), (Z_{tt} = Z_{rr}) \tag{8.25}$$

Embedding the α and γ segment equations (8.24) and (8.25), in a partitioned form, gives

$$\begin{bmatrix} V_q \\ V_s \end{bmatrix} = -\begin{bmatrix} Z_{rr} & 0 \\ 0 & Z_{rr} \end{bmatrix}\begin{bmatrix} i_q \\ i_s \end{bmatrix} \tag{8.26}$$

Similarly, equations (8.22), (8.23) can be put in the partitioned form

$$\begin{bmatrix} V_q \\ V_s \end{bmatrix} = \begin{bmatrix} Z_{qq} & Z_{qs} \\ Z_{qs} & Z_{qq} \end{bmatrix}\begin{bmatrix} i_q \\ i_s \end{bmatrix} + \begin{bmatrix} Z_{qp} \\ Z_{sp} \end{bmatrix} i_p \tag{8.27}$$

For equation (8.21) to be conformable with equations (8.26) and (8.27) it is necessary to write this equation in the partitioned form

$$V_p = Z_{pp}i_p + \begin{bmatrix} Z_{pq} & Z_{ps} \end{bmatrix}\begin{bmatrix} i_q \\ i_s \end{bmatrix} \tag{8.28}$$

Equations (8.26), (8.27), (8.28) constitute the three equations to be solved for the input impedance, V_p/i_p.

Equating equations (8.26), (8.27), gives

$$-\begin{bmatrix} Z_{rr} & 0 \\ 0 & Z_{rr} \end{bmatrix}\begin{bmatrix} i_q \\ i_s \end{bmatrix} = \begin{bmatrix} Z_{qq} & Z_{qs} \\ Z_{qs} & Z_{qq} \end{bmatrix}\begin{bmatrix} i_q \\ i_s \end{bmatrix} + \begin{bmatrix} Z_{qp} \\ Z_{sp} \end{bmatrix} i_p \tag{8.29}$$

from which,

$$\begin{bmatrix} i_q \\ i_s \end{bmatrix} = -\begin{bmatrix} Z_{rr}+Z_{qq} & Z_{qs} \\ Z_{qs} & Z_{rr}+Z_{qq} \end{bmatrix}^{-1} \begin{bmatrix} Z_{qp} \\ Z_{sp} \end{bmatrix} i_p \tag{8.30}$$

Substituting, $\begin{bmatrix} i_q & i_s \end{bmatrix}^T$ from equation (8.30) into equation (8.29), then gives

$$V_p = Z_{pp} i_p - \begin{bmatrix} Z_{pq} & Z_{ps} \end{bmatrix} \begin{bmatrix} Z_{rr}+Z_{qq} & Z_{qs} \\ Z_{qs} & Z_{rr}+Z_{qq} \end{bmatrix}^{-1} \begin{bmatrix} Z_{qp} \\ Z_{sp} \end{bmatrix} i_p \tag{8.31}$$

hence, an explicit matrix input impedance formula is given by

$$Z_{in} = \frac{V_p}{i_p} = Z_{pp} - \begin{bmatrix} Z_{pq} & Z_{ps} \end{bmatrix} \begin{bmatrix} Z_{qq}+Z_{rr} & Z_{qs} \\ Z_{qs} & Z_{qq}+Z_{rr} \end{bmatrix}^{-1} \begin{bmatrix} Z_{pq} & Z_{ps} \end{bmatrix}^T. \tag{8.32}$$

A MathCAD program listing for the above input impedance evaluation is given in *Appendix 8B.*

8.7 Comparison of Measured, Simulated and Predicted Results for the Antenna

For the antenna, *E*, a simulated *Q*-factor of 500 was used. For the first mode frequency, f_1, the current density distribution is maximum in the horizontal β segment of the antenna, so a 50 Ω input impedance will be found in this segment. By trial calculation using equation (8.32) for Z_{in}, a probe feed position was found at x_p=4.2 mm, y_p=6 mm (Figure 8.19(b)), giving a close match to 50 Ω at the operating frequency, f_1. This formula is useful in the trial-and-error optimum design because of the short computer time required. The elements in the coupling impedance matrices, Z_{pq}, Z_{pp} in equation (8.32), for Z_{in}, are evaluated using the equations (7.23), (7.29), given in Chapter 7. The matrix elements in Z_{qq}, Z_{rr} and Z_{qs} for the α and β segments were evaluated using equations (6.14), (6.17), given in Chapter 6. The antenna with the computed probe feed location was modelled, and, fabricated, as shown in Figure 8.20.

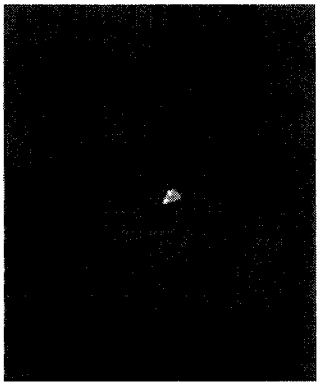
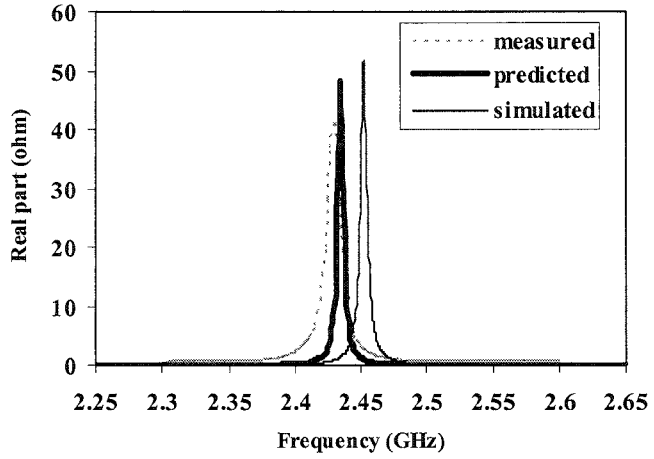
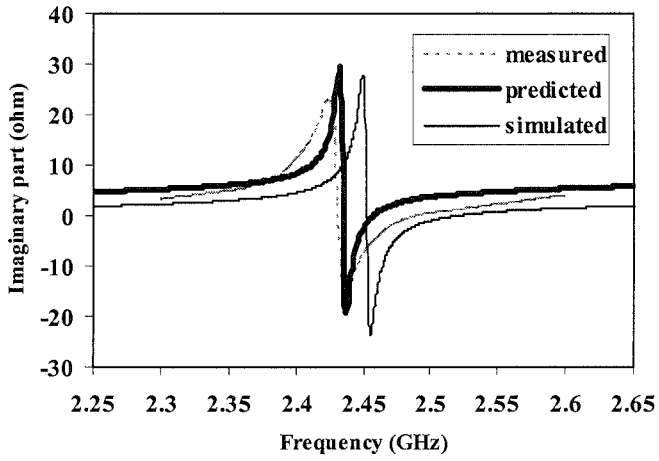


Figure 8.20: Fabricated H-shaped antenna for a 50 Ω match.

The predicted, simulated and measured input impedance and return loss are shown in Figures 8.21 and 8.22.



(a)



(b)

Figure 8.21: Predicted, simulated and measured Z_{in}. (a) Real part. (b) Imaginary part.

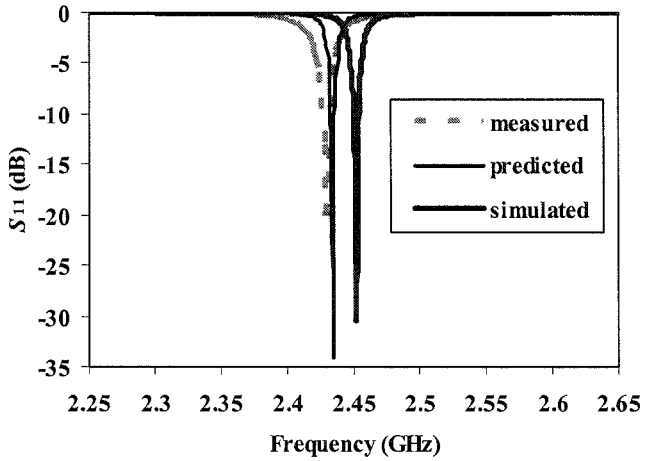


Figure 8.22: Predicted, simulated and measured S_{11}.

As shown in Figures 8.21 and 8.22, good agreement between the predicted, simulated and measured results is obtained for the input impedance, Z_{in} and return loss, S_{11}. The calculated, simulated and measured input impedances are 48.3 Ω at 2.435 GHz, 51.8 Ω at 2.452 GHz and 42+j2.7 Ω at 2.43 GHz and the calculated, simulated and measured S_{11} are -34 dB at 2.435 GHz, -31 dB at 2.452 GHz and -20 dB at 2.43 GHz.

Measured and simulated gain is shown in Figure 8.23, where a measured gain of 3.73 dBi was obtained at 2.43 GHz.

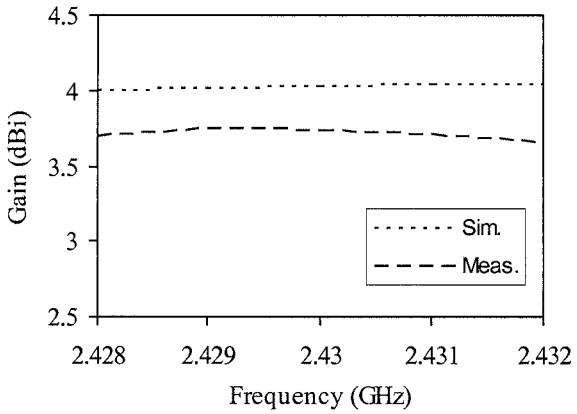


Figure 8.23: Measured and simulated gain.

The measured E-plane and H-plane radiation patterns at 2.43 GHz are shown in Figures 8.24 and 8.25. The cross-polarisation levels are 27 dB and 28.5 dB below the co-polarisation component at boresight for E-plane and H-plane.

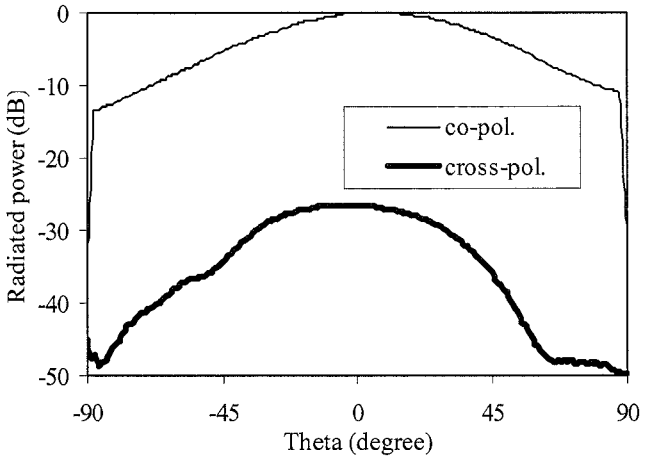


Figure 8.24: Measured E-plane radiation pattern at 2.43 GHz.

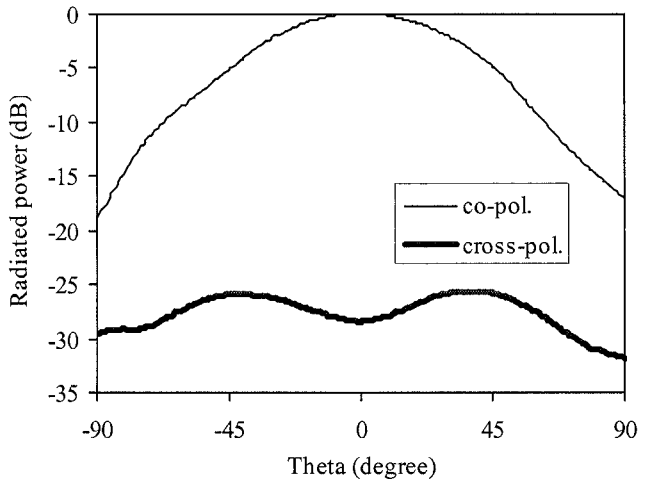


Figure 8.25: Measured H-plane radiation pattern at 2.43 GHz.

8.8 Summary

Using odd and even mode conditions four mode frequency formulas are derived with a new and simpler formula for the fourth mode frequency being obtained. Empirical parametric studies have been employed to obtain value for W_a for the three ratios W_2/W_1

which gave accurate prediction at the first mode frequency, f_1. Also, the number of unknown design parameters has been reduced to three. For each of the three ratios, W_2/W_1, good agreement is obtained between the predicted, simulated and measured values for the four mode frequencies.

Using the above empirical parametric studies and employing a two dimensional contour plot, a design strategy is presented for the design of an antenna operating at a given fundamental mode frequency, f_1. Again, good agreement has been obtained between the predicted, simulated and measured results for the designed antennas.

A new explicit matrix input impedance formula for the H-shaped microstrip patch antenna has been obtained using segmentation method. Applying the new matrix input impedance formula, the location of the probe feed for a $50\ \Omega$ match was located. The predicted and simulated values of input impedance and return loss for the H-shaped antenna show good agreement with the measured results.

The simple mode frequency formulas, and the explicit probe feed matrix input impedance formula, were used in the proposed design approach to design an H-shaped microstrip patch antenna to operate at a pre-assigned frequency.

CHAPTER 9 A NEW APPROACH TO THE DESIGN OF A COMPACT HIGH EFFICIENCY ACTIVE INTEGRATED ANTENNA

9.1 Introduction

A block diagram of a conventional transmitter front-end shown in Figure 9.1 which consists of an output matching network, a harmonic matching network, an antenna matching network and an interconnecting cable between the PA and antenna.

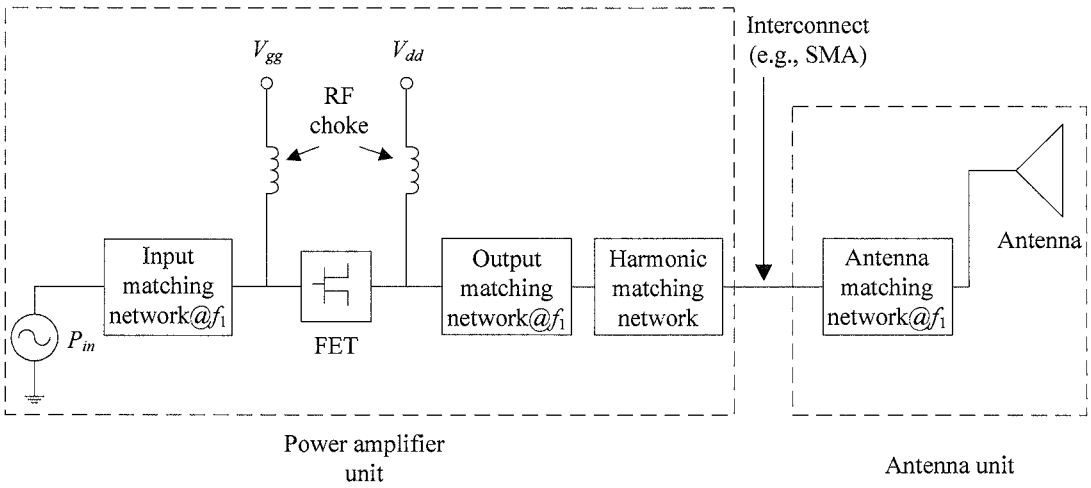


Figure 9.1: Block diagram of a conventional transmitter front-end.

By the use of a high efficiency PA the size of a conventional transmitter can be reduced and also a smaller size battery power source is required. Further size reduction can be obtained by using an AIA approach where the output matching network, harmonic matching network, antenna matching network and interconnecting cable are all eliminated [7]. An additional advantage of the AIA design approach is that as extra space is available so it is possible to include further multi-function applications.

In this chapter, an H-shaped patch antenna is used in the AIA design. This antenna was chosen because of its compact size and its ability to suppress the PA's second and

third harmonics by optimising the patch dimensions and appropriate location of the probe feed.

For the AIA two designs are presented. In the first AIA design (see Figure 9.2) a probe feed position on the antenna is found to give an input impedance of 50 Ω and also to suppress the second and third mode frequencies. For this structure an antenna matching network is not needed. This AIA achieved a peak PAE of 67.5% and a P_{out} of 21.69 dBm.

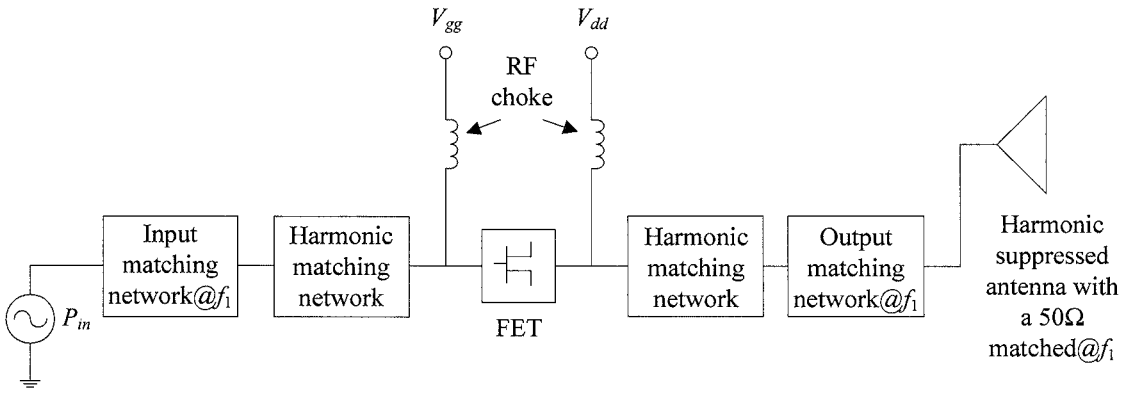


Figure 9.2: Block diagram of a proposed AIA circuit using a conventional approach.

In the second design a further size reduction of the transmitter is obtained by connecting the antenna directly to the active device as shown in Figure 9.3.

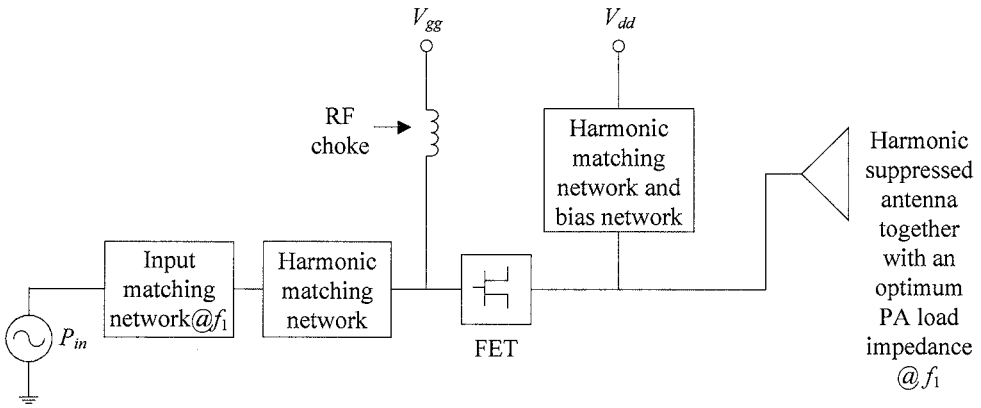


Figure 9.3: Block diagram of a proposed AIA circuit using a new approach.

For high frequency PAs the drain bias network (RF choke) is normally replaced by a quarter wavelength transmission line. In this design the length of this line and the probe feed position are employed to obtain the required optimum load impedances at the fundamental frequency and second harmonic. Consequently the load matching network shown in Figure 9.2 is not used and the size of the transmitter is further reduced. As this design reduces the number of components in the circuit the losses are also reduced. A measured peak PAE of 68.2% with a 21.81 dBm P_{out} was obtained. Full details of the two designs are given in Sections 9.3, 9.4 and 9.5 of this chapter together with simulated and practical results.

9.2 Literature Survey of AIA

Radisic has proposed three novel architectures for the realisation of an AIA. In [137] a class-B PA operating at 2.48 GHz was integrated with a rectangular patch antenna where shorting pins were located at the middle of the antenna to suppress the second harmonic. This design produced a PAE of 55%. For the second AIA design [138] Radisic used a circular sector patch antenna. The resonant frequencies of the antenna are given by the roots of a Bessel function involving the antenna dimensions which can be optimised to suppress the second and third harmonics. This antenna was then integrated with a class-F PA and a PAE of 63% obtained. For the third AIA design in order to obtain broadband operation, a broader bandwidth slot antenna combined with a periodic structure based on the photonic band gap (PBG) was used to provide broadband harmonic tuning at the second harmonic [139]. The maximum efficiency was 61% and an 8% bandwidth over a 50% PAE was achieved. In [107], [140], Chung successfully used a high breakdown voltage active device and a circular sector patch antenna in the AIA design where the antenna acts as both the radiator and output harmonic tuner. Two AIA circuits were designed and a peak PAE of 55% was obtained at 2.45 GHz and a peak PAE of 42%

obtained at 7.25 GHz. In all of the above AIA designs an output matching network was needed to obtain maximum output power and efficiency at the operating frequency.

Deal [141] proposed two AIA designs, one for narrow bandwidth efficiency and the other for wideband efficiency. In the first AIA design a dual feed rectangular patch antenna was integrated with a push-pull PA where a PAE of 55% at 2.5 GHz was obtained. In the second AIA design in order to increase the efficiency bandwidth the rectangular patch antenna was replaced by a slot antenna and a PAE of 63% at 2.46 GHz with an 8% bandwidth for efficiency of over a 55% was obtained. For the design frequency of 4.15 GHz Hang [142] used a push-pull PA to feed a modified unipolar quasi-yagi antenna and produced a PAE of 60.9%. Recently Lee [143] has proposed a new non-contact differential fed antenna where a class-B push-pull PA was used and PAE of 29% was obtained at 2.64 GHz.

In [144] a two-layer planar inverted-F antenna (PIFA) was used as a load for a class-F PA. Two shorting pins, a probe feed pin and a short section of transmission line were used to obtain an optimum load at the fundamental frequency, a short circuit at the second harmonic and an open circuit at the third harmonic terminations. Three AIA were designed and the PAEs obtained at 1.05 GHz, 1.55 GHz and 1.8 GHz were 58%, 52% and 50%.

For a class-E PA Weiss [145] eliminated the output matching network by the use of a slot antenna connected directly to the active device. The antenna was designed to produce the required optimum load impedance at the fundamental frequency and an open circuit termination at the second harmonic. A PAE of 62% was obtained at 10 GHz. Kim [7] also proposed direct integration of a slot antenna for a class-F PA operating at 5.5 GHz. The antenna was optimised to provide an optimum load impedance at the fundamental frequency, a short circuit termination at the second harmonic, and an open circuit termination at the third harmonic. A PAE of 67.5% was obtained.

In the above designs [7], [144], [145] optimum loads for the second harmonic (short circuit) and third harmonic (open circuit) were obtained on the assumption that the active device behaved as a lossless switch. Consequently optimum efficiency was not obtained as the effect of the active device parasitics was not included in the design. Colantonio [146] included the effects of the parasitics and obtained the optimum load impedances for the PA at the fundamental frequency, second and third harmonics. An inset feed rectangular patch with shorting pins was designed to produce an optimum impedance at the fundamental frequency, and low second and third harmonics impedances. However an output matching network was added between the antenna and the PA to transform the patch's second and third harmonic impedances to the required optimum values for maximum efficiency. Simulated result showed a maximum PAE of about 60% at 5 GHz.

In all of the above AIA designs the approach for improving the efficiency was wholly focused on the load harmonic terminations and a conjugate match was obtained at the source port for the fundamental frequency only. To date no research work has been reported on the use of source harmonic matching network for the AIA design. In this chapter, the source and load harmonic matching networks are used in order to maximise the efficiency of the AIA.

9.3 Two Designs of AIA Using the H-shaped Patch Antenna

In this section, a compact H-shaped patch antenna is used as an output load for the active device. In the first AIA design a probe feed position of the antenna was found to ensure that the antenna did not radiate power at the second and third harmonics of the PA and with an input impedance of 50 Ω at the fundamental frequency. Consequently, the class-F PA circuit designed in Chapter 5 (see Section 5.6) was used in which the antenna simply replaced the 50 Ω load. In the second AIA design, the load matching network was eliminated by finding a probe feed position to obtain an optimum impedance at the

fundamental frequency. Also the drain bias network was used to obtain an optimum impedance at the second harmonic.

In the first AIA design the antenna E (see Chapter 8) operating at a first mode frequency of 2.45 GHz with an input impedance of 50 Ω was used. The geometry of this antenna and probe feed location is shown in Figure 9.4 with the dimensions given in Table 9.1.

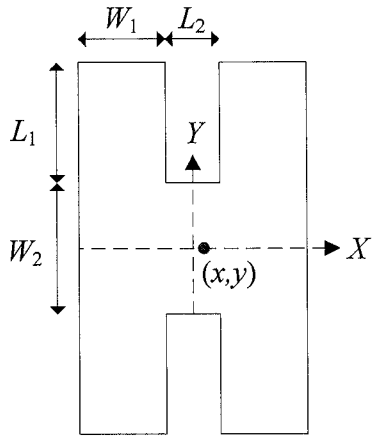


Figure 9.4: Geometry of the antenna.

W_1 (mm)	W_2 (mm)	L_1 (mm)	L_2 (mm)	x, y (mm)
8	12	12.35	5.2	12.2, 18.3

Table 9.1: Dimensions and probe feed locations, (x, y) for antenna E.

It was shown that with the above dimensions and feed position the following results were obtained.

1. At the first mode frequency, f_1, an input impedance of close to 50 Ω was obtained.
2. The two mode frequencies, f_2, f_3 of the antenna are suppressed.
3. The antenna's fourth mode frequency, f_4 is different from the PA's second and third harmonics.

The simulated frequency response of the input impedance for this antenna is shown in Figure 9.5. The input impedance at the four mode frequencies (f_1, f_2, f_3, f_4) and the first two harmonics ($2f_1$, $3f_1$) is given in Table 9.2.

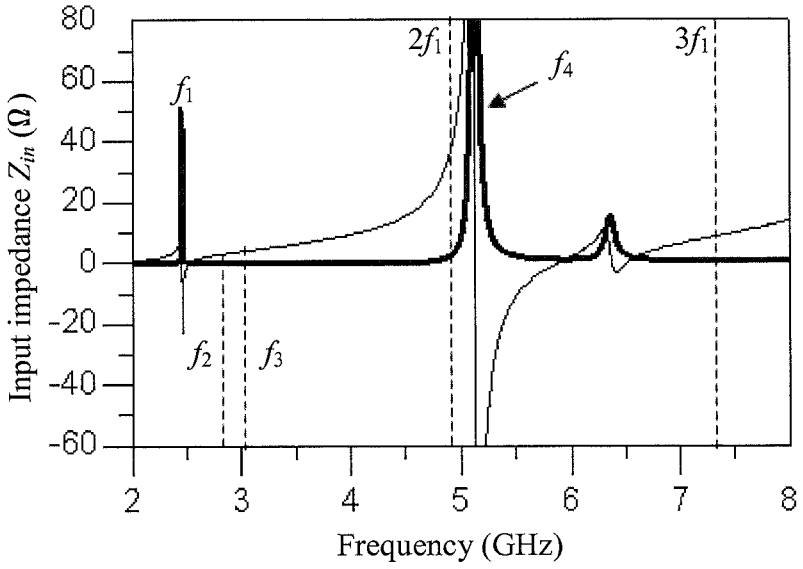


Figure 9.5: Simulated impedance response of the antenna *E* with x=12.2 mm, y=18.3 mm.

Mode	f_1	f_2	f_3	$2f_1$	$3f_1$
Z_{in} (Ω)	51.8	$j3$	$j4$	2+j35	0.7+j9

Table 9.2: Simulated input impedance at key frequencies.

For the second AIA design, the dimensions of the antenna were the same as given in Table 9.1. To obtain the optimum impedance (Z_{in}=36-j7) at the first mode frequency f_1 the probe feed location was changed to x=12 mm, y=18.3 mm. The simulated frequency response of the input impedance is shown in Figure 9.6 and the simulated values of input impedance at the key frequencies are given in Table 9.3.

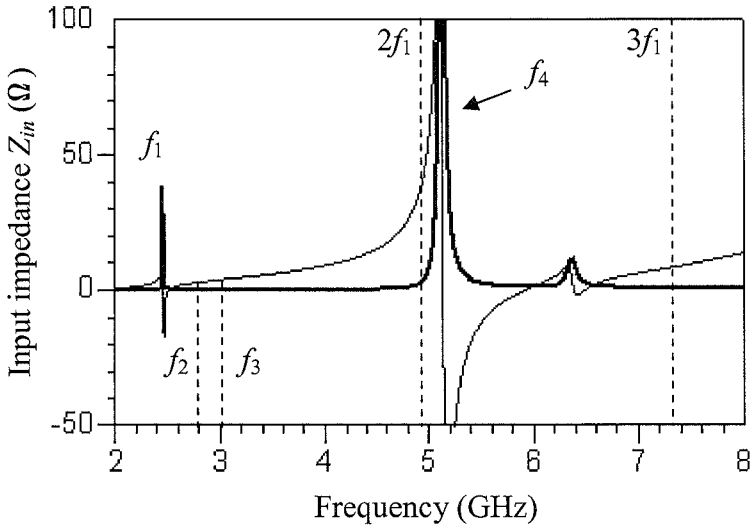


Figure 9.6: Simulated impedance response of the antenna *E* with x=12 mm, y=18.3 mm.

Mode	f_1	f_2	f_3	$2f_1$	$3f_1$
Z_{in} (Ω)	36-j7	j3	j4	2+j35	0.7+j9

Table 9.3: Simulated input impedance at key frequencies.

In an AIA circuit the output power from the PA can not be directly measured using a spectrum analyser, or, power meter. The power gain was therefore measured in an anechoic chamber as shown in Figure 9.7.

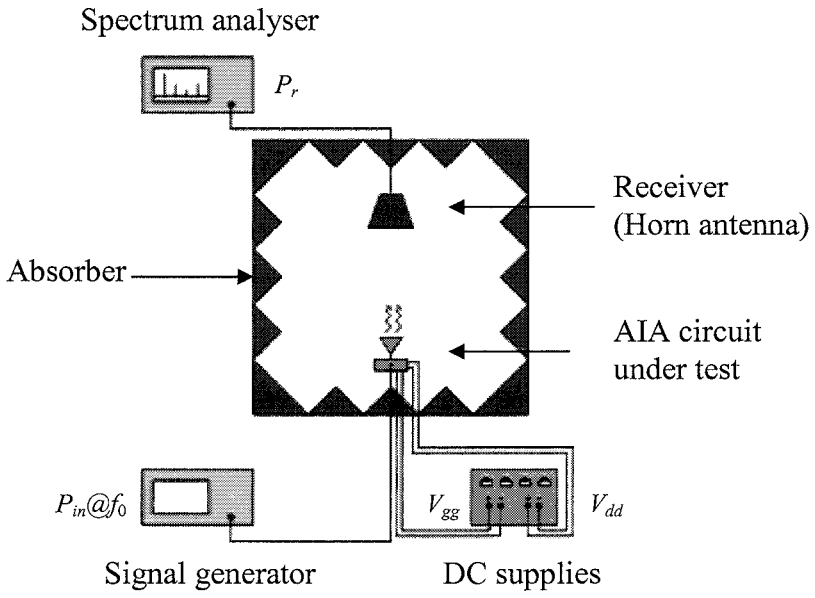


Figure 9.7: Measurement setup for an AIA circuit.

The received radiated powers, P_r from the AIA and from an identical passive antenna without the PA were measured over a range of input power P_{in}. The difference in the two received radiated powers is a measure of the gain of the PA alone. The PAE and the P_{out} of the PA are obtained using equations (9.1) and (9.2) given below.

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \tag{9.1}$$

and,

$$P_{out} = G_p P_{in} \tag{9.2}$$

The radiation patterns at the E- and H-planes for the AIA circuit were also measured to ensure that there are no adverse radiation effects directly from the PA.

9.4 AIA Using Antenna and Load/Source Harmonic Matching Networks

Figure 9.8 shows a complete circuit of the AIA where the antenna is modelled as a single port network and the same load/source matching networks which were designed in Chapter 5 are used.

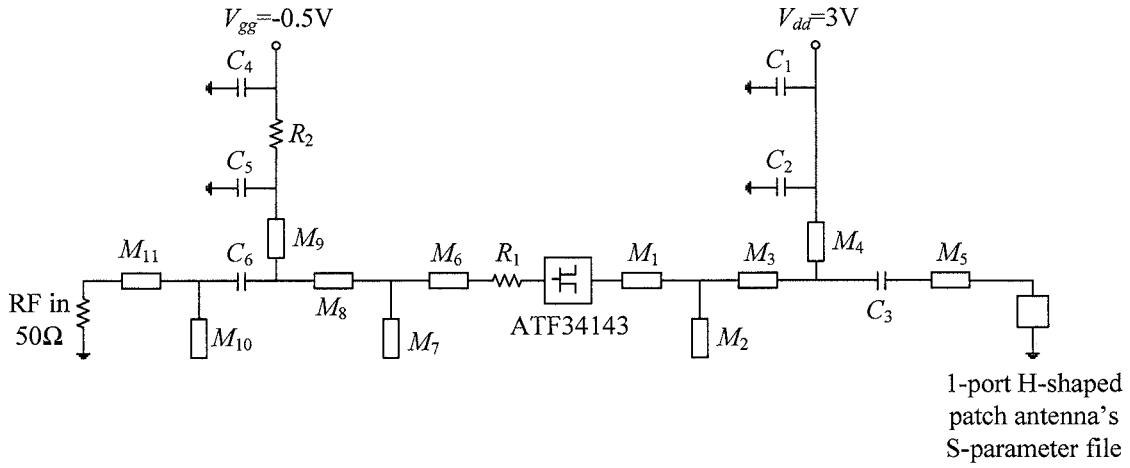


Figure 9.8: Circuit diagram of the AIA circuit.

The optimum harmonic impedances obtained by the load/source-pull method together with those obtained for the AIA circuit shown in Figure 9.8 are compared in Table 9.4. As can

be seen there is a close agreement between the two sets of values showing that mode impedances of the antenna have negligible effects on the required harmonic impedances.

	Load/source impedance, $Z_L(\Omega)$, $Z_S(\Omega)$ obtained by load/source-pull method	Load/source impedance, $Z_L(\Omega)$, $Z_S(\Omega)$ obtained for the AIA circuit
Z_{L1}	36-j7	38-j7
Z_{L2}	2-j61	6-j66
Z_{L3}	1+j148	2+j171
Z_{S2}	5-j30	11.5-j39
Z_{S3}	50+j220	51+j240

Table 9.4: Simulated load and source impedances at P_{in}=13 dBm.

Figure 9.9 shows that the overlapping area between the drain current and voltage waveforms is small and therefore high efficiency is obtained for the designed AIA circuit.

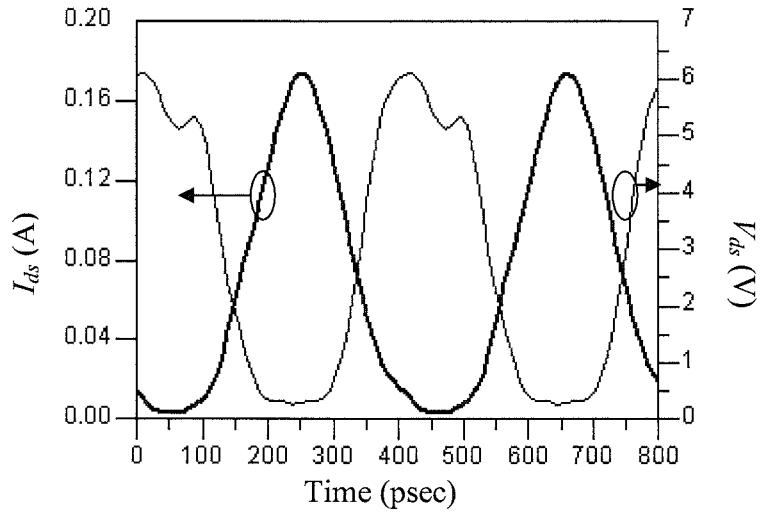


Figure 9.9: Simulated V_{ds} and I_{ds} waveforms at 2.45 GHz with P_{in}=9 dBm (2.1-dB compression).

Figure 9.10 shows the frequency response for an S_{11} where an S_{11} of -27 dB is obtained at the design frequency f_1.

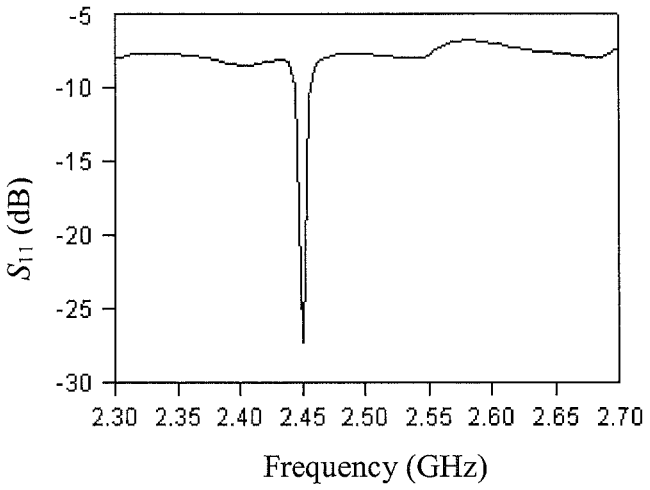


Figure 9.10: Simulated S_{11} at P_{in}=9 dBm .

Figure 9.11 shows that a good harmonic suppression at the second and third harmonics has also been obtained.

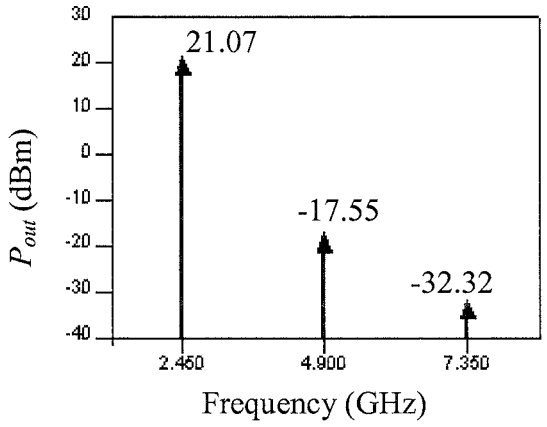
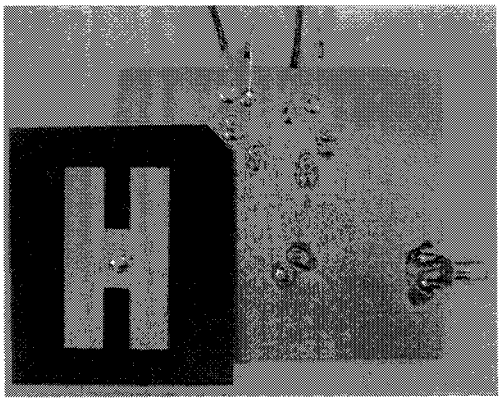
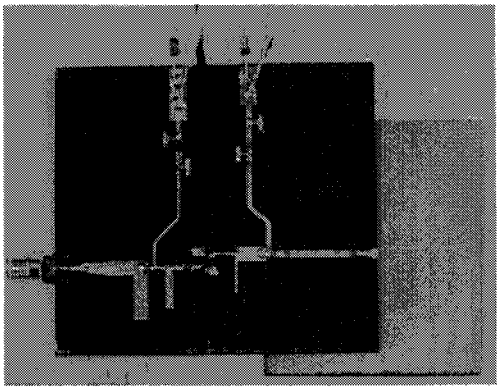


Figure 9.11: Simulated P_{out} spectrum at P_{in}=9 dBm.

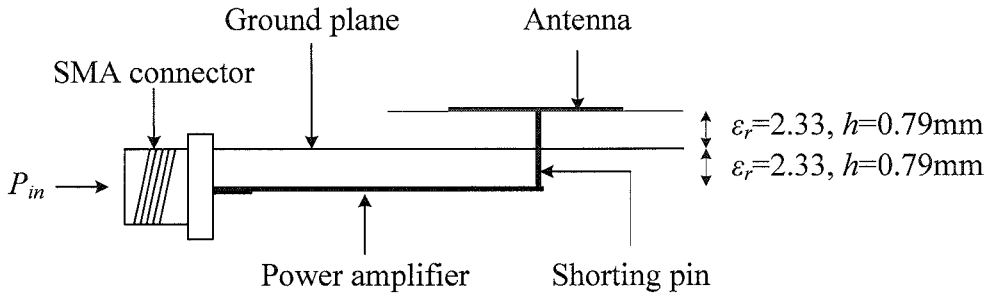
The AIA circuit was realised using a Duroid substrate with a thickness of 0.79 mm. The PA circuit was placed on the lower surface and the antenna was placed on the upper side of the substrate as shown in Figures 9.12(a) and (b). A side view of the AIA circuit is shown in Figure 9.12(c).



(a)



(b)



(c)

Figure 9.12: Photograph of the fabricated AIA circuit. (a) Top view. (b) Bottom view. (c) Schematic diagram.

The measured and simulated response of P_{out}, G_p, and, PAE as a function of P_{in} are shown in Figures 9.13 and 9.14.

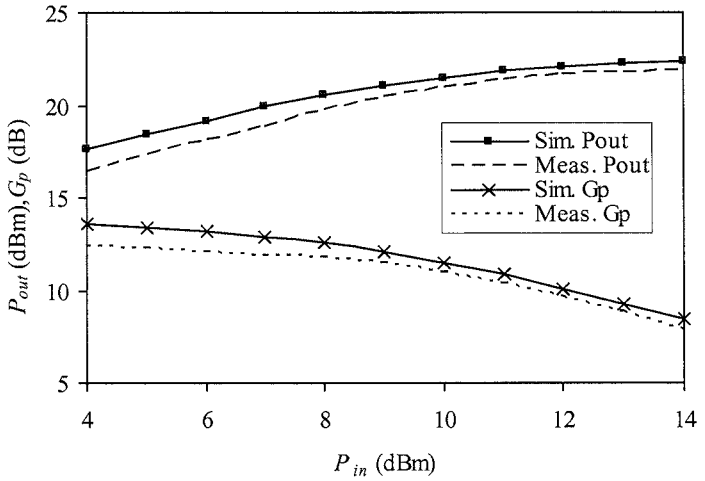


Figure 9.13: Simulated and measured G_p and P_{out} as a function of P_{in} at 2.428 GHz.

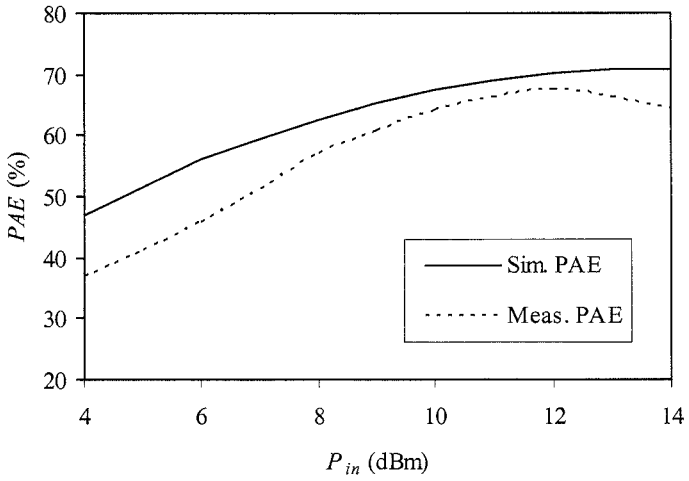


Figure 9.14: Simulated and measured PAE as a function of P_{in} at 2.428 GHz.

The measured peak PAE was 67.5% with a P_{out} of 21.69 dBm was achieved at a low drain voltage V_{dd} of 3 V and a P_{in} of 12 dBm at 2.428 GHz. Compared with the PAE obtained in Chapter 5 (70.4%) there has been a reduction of 2.9% which is the result of power lost at the higher mode frequencies of the antenna, and, measurement errors.

The measured E-plane and H-plane radiation patterns for passive and active antennas at 2.428 GHz are compared in Figures 9.15 and 9.16.

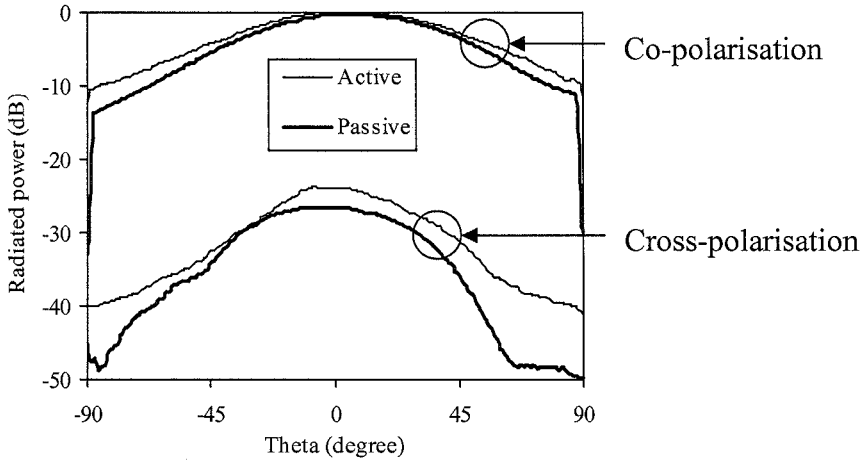


Figure 9.15: Measured E-plane radiation patterns at 2.428 GHz.

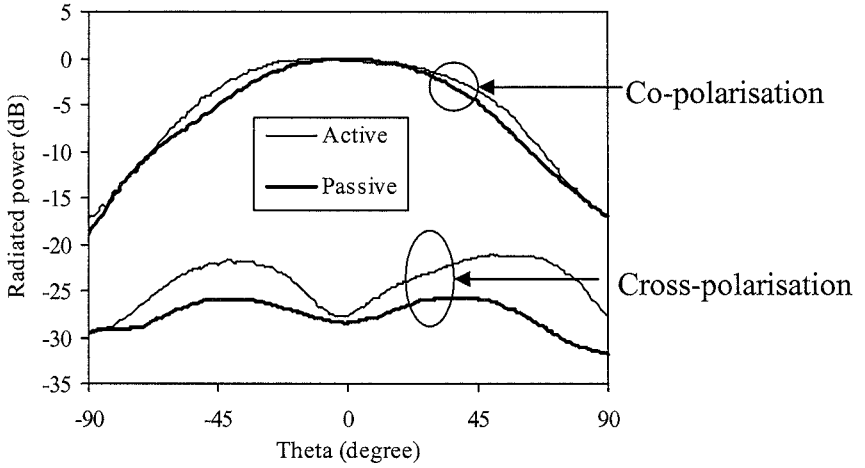


Figure 9.16: Measured H-plane radiation patterns at 2.428 GHz.

Good agreement has been obtained between the passive and active antennas. The cross-polarisation levels for the active antenna are 24 dB and 27.7 dB below the co-polarisation component at bore sight for E- and H-planes.

9.5 New Approach to the Design of an AIA

A more compact form of an AIA circuit is obtained, by eliminating the load matching network using a probe feed to obtain the optimum impedance at the fundamental

frequency, and, by designing the drain bias network to obtain the required optimum impedance at the second harmonic. The designed AIA circuit is shown in Figure 9.17.

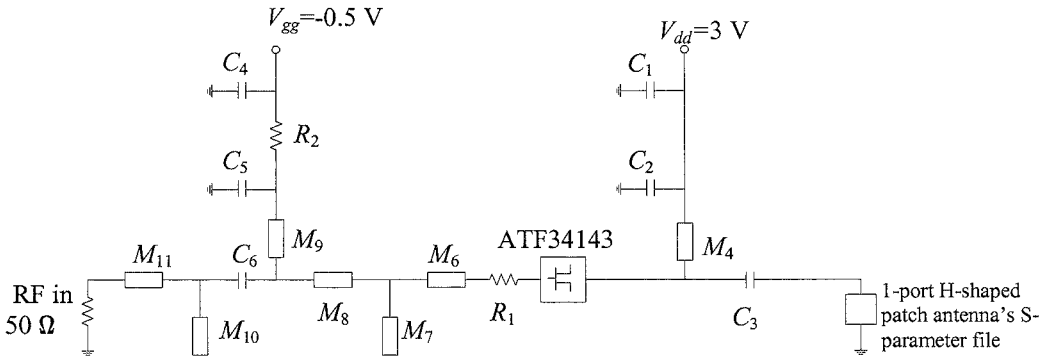


Figure 9.17: Circuit diagram of the AIA circuit.

In the previous AIA circuit, the lines M_3, M_4 (see Figure 9.8) were used to obtain the optimum load impedance at the second harmonic. In the new design this is achieved by eliminating M_3 and determining the required length θ_4 of M_4 as shown in Figure 9.18.

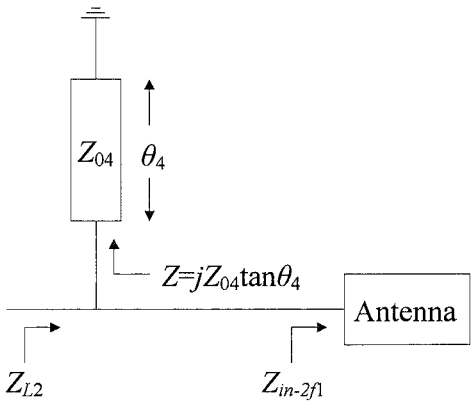


Figure 9.18: AC equivalent circuit of the load network.

The impedance Z_{L2} at the second harmonic is given by equation (9.3).

$$Z_{L2} = \frac{jZ_{04}\tan\theta\, Z_{in\_2f1}}{jZ_{04}\tan\theta + Z_{in\_2f1}} \tag{9.3}$$

where, Z_{L2}=-j61 Ω (see Table 9.4), the input impedance of the antenna at the second harmonic Z_{in_2f1} is j35 Ω (see Table 9.3) and Z_{04}=100 Ω.

The value of θ_4 (=83.7°) is obtained using equation (9.4).

$$\theta_4 = \frac{1}{2}\left(\pi + \tan^{-1}\left(\frac{j}{Z_{04}}\frac{Z_{L2}Z_{in\_2f1}}{Z_{L2} - Z_{in\_2f1}}\right)\right) \tag{9.4}$$

The frequency response for the network (see Figure 9.18) is shown in Figure 9.19 and as can be seen the required value of Z_{L2} has been obtained.

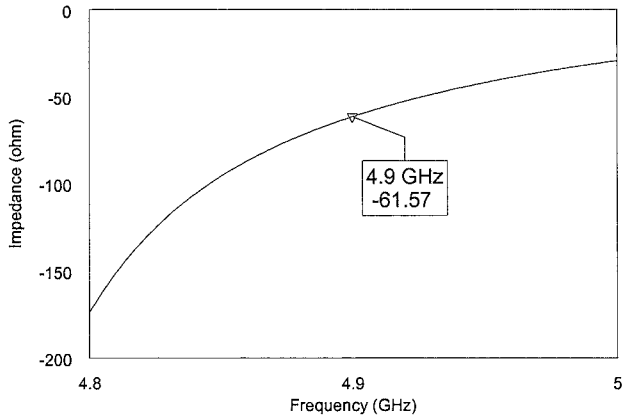


Figure 9.19: Simulated load impedance response.

The drain voltage/current waveforms (see Figure 9.20) show small overlap between drain voltage and current waveforms and so high PAE is obtained.

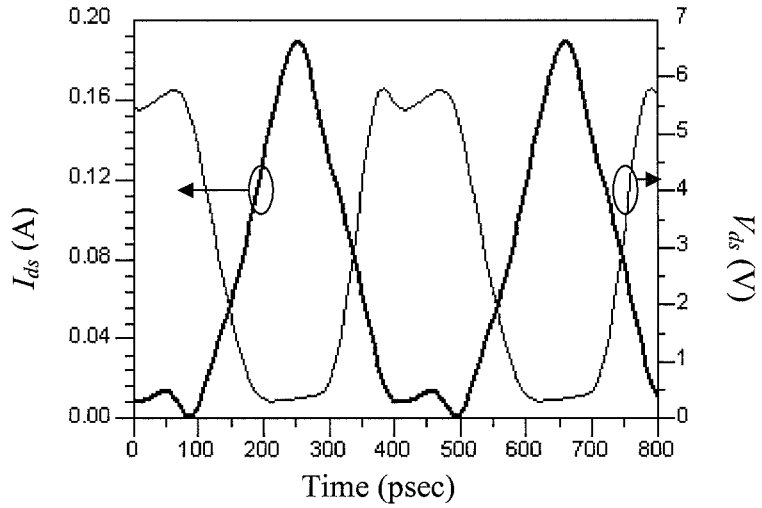


Figure 9.20: Simulated V_{ds} and I_{ds} waveforms at 2.45 GHz with P_{in}=9 dBm (2-dB compression).

Figure 9.21 show that good matching (S_{11}=-24 dB) has been obtained at the design frequency while Figure 9.22 shows good harmonic suppression at the second and third harmonics.

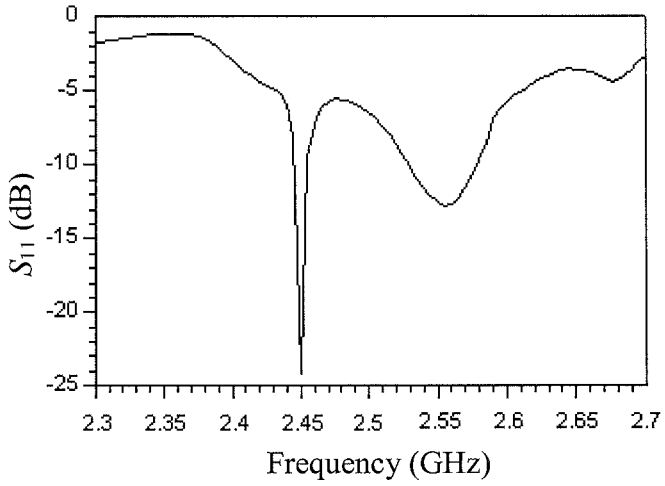


Figure 9.21: Simulated S_{11} at P_{in}=9 dBm.

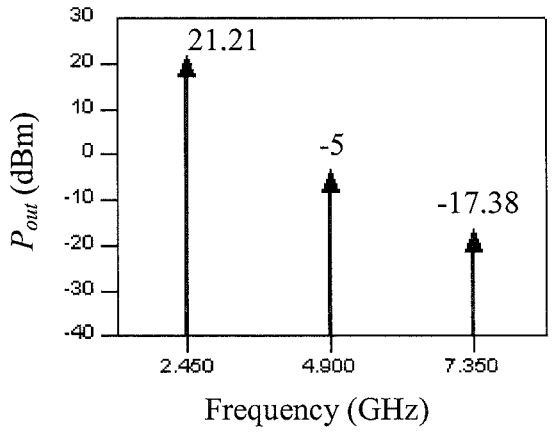
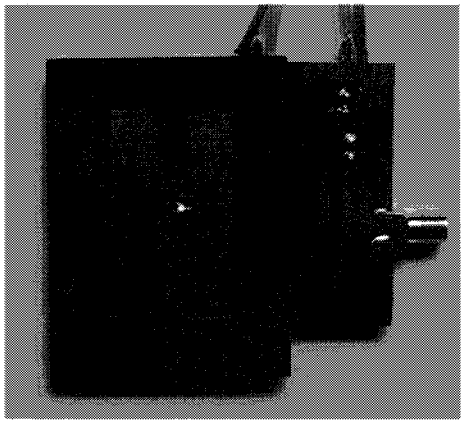
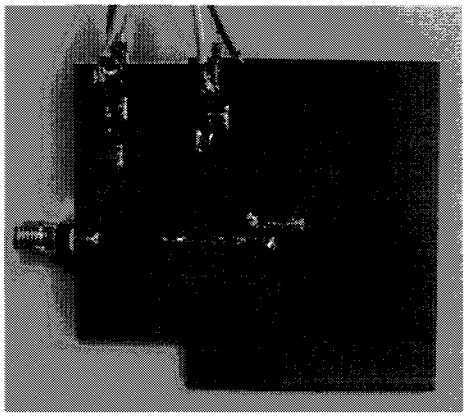


Figure 9.22: Simulated P_{out} spectrum at P_{in}=9 dBm.

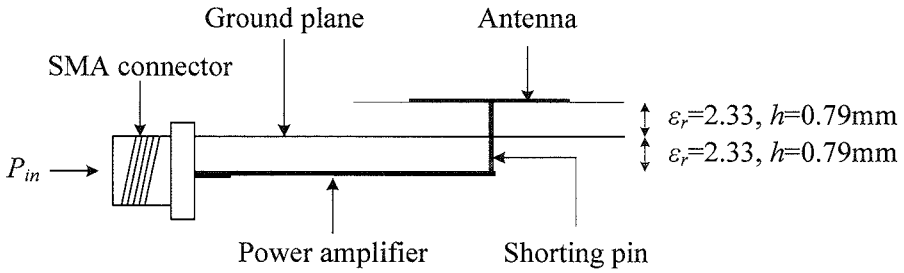
The fabricated AIA circuit is shown in Figure 9.23.



(a)



(b)



(c)

Figure 9.23: Photograph of the fabricated AIA circuit. (a) Top view. (b) Bottom view. (c) Schematic diagram.

Measured and simulated PAE, P_{out} and G_p performances as a function of P_{in} are shown in Figures 9.24 and 9.25. The measured peak PAE was improved to 68.2%, and the P_{out} improved to 21.81 dBm for a P_{in} of 12 dBm at 2.431 GHz.

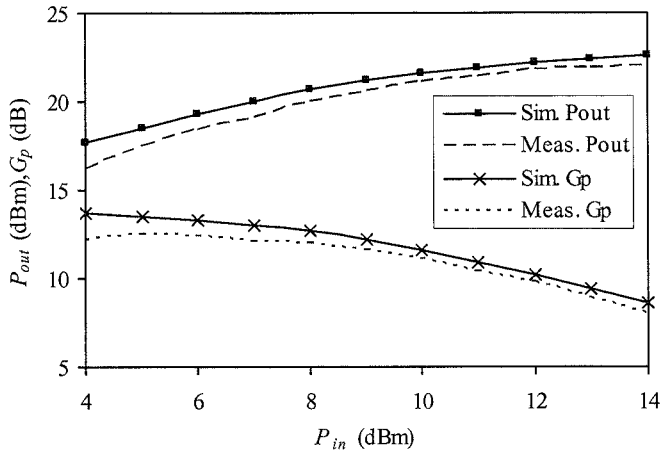


Figure 9.24: Simulated and measured G_p and P_{out} as a function of P_{in} at 2.431 GHz.

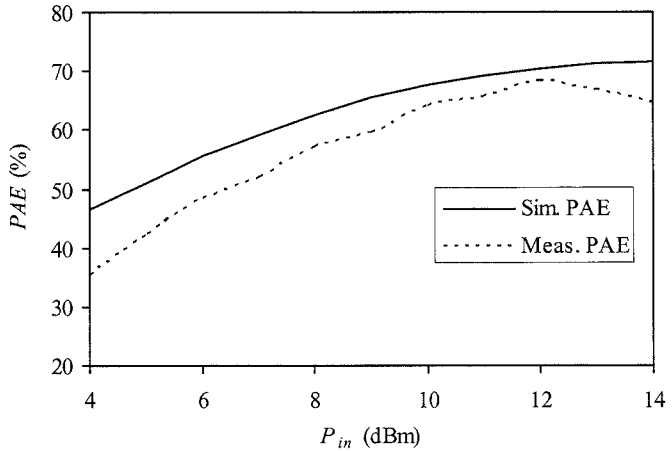


Figure 9.25: Simulated and measured PAE as a function of P_{in} at 2.431 GHz.

The measured E-plane and H-plane radiation patterns for passive and active antennas at 2.431 GHz are compared in Figures 9.26 and 9.27.

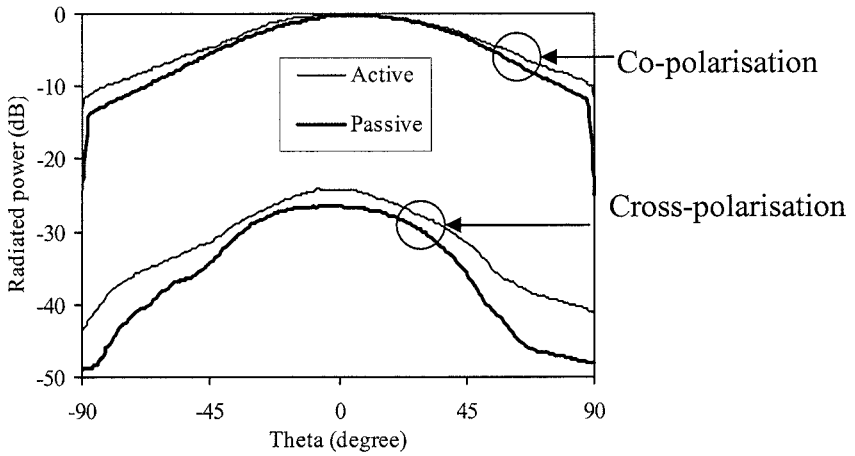


Figure 9.26: Measured E-plane radiation patterns at 2.431 GHz.

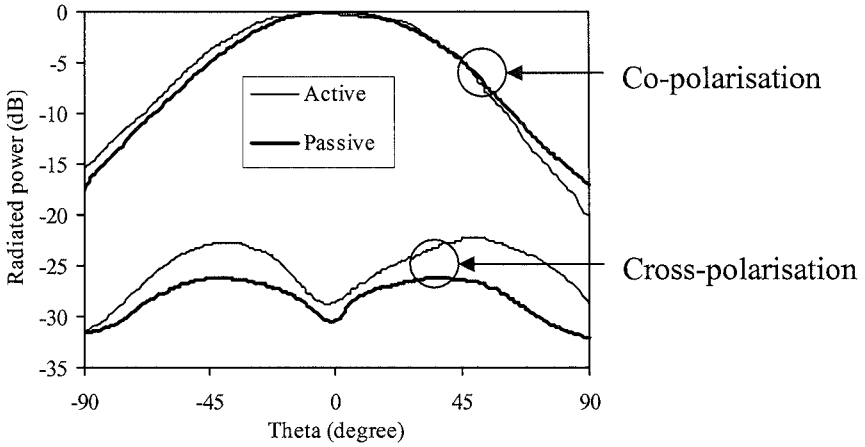


Figure 9.27: Measured H-plane radiation patterns at 2.431 GHz.

The active antenna has similar radiation patterns to that of the passive antenna. Cross-polarisation levels for the active antenna are 24.3 dB and 28.7 dB below the co-polarisation component at bore sight for E- and H-planes.

9.6 Summary

Two AIA circuits operating at 2.45 GHz have been designed. In the first AIA design a conventional approach was used to integrate a PA with a 50 Ω matched antenna. The load matching network was designed so that the 50 Ω passive load in the PA circuit could be replaced by the antenna. A measured PAE of 67.5% and a very good harmonic suppression at the second and third harmonics was obtained. In the second AIA design, in order to further minimise the size, cost, and losses, direct integration between the antenna and the PA has been proposed. For this design optimum load impedances at the fundamental frequency and second harmonic were obtained by adjusting the probe feed position and the length of the drain bias network. An increased in PAE to 68.2% was obtained which is slightly higher than for the first AIA design.

The results obtained in this chapter compare favourably with published work as can be seen in the following tables.

Reference	PA Mode Operation	Antenna type (Linear polarisation)	f_1 (GHz)	P_{out} (dBm)	PAE (%)
[137]	class B	Modified rectangular patch antenna with shorting pin	2.48	31.6	55
[138]	class F	Circular sector patch	2.55	24.4	63
[139]	class F	Modified rectangular patch with shorting pin and PBG	2.45	21.9	61
[141]	Push-pull	Dual feed patch	2.46	26	63
[141]	Push-pull	Dual feed slot	2.5	25	55
[144]	class F	PIFA	1.05	25.3	58
[144]	class F	PIFA	1.55	26.3	52
[144]	class F	PIFA	1.8	25	50
This work (Section 9.4)	class F	H-shaped patch	2.45	21.69	67.5
This work (Section 9.5)	class F	H-shaped patch	2.45	21.81	68.2

Table 9.5: Performances of GaAs FET AIA circuit operating at L- and S-bands.

Reference	Antenna type (Linear polarisation)	f_1 (GHz)	P_{out} (dBm)	PAE (%)
[138]	Circular sector patch	2.55	24.4	63
[139]	Modified rectangular patch with shorting pin and PBG	2.45	21.9	61
[140]	Circular sector patch	2.45	30	55
[107]	Circular sector patch	7.25	30.3	42
[144]	PIFA	1.05	25.3	58
[144]	PIFA	1.55	26.3	52
[144]	PIFA	1.8	25	50
[7]	Slot	5.5	27.23	67.5
This work (Section 9.4)	H-shaped patch	2.45	21.69	67.5
This work (Section 9.5)	H-shaped patch	2.45	21.81	68.2

Table 9.6: Performances of GaAs FET class-F AIA circuit.

CHAPTER 10 CONCLUSIONS AND FURTHER WORK

10.1 Conclusions

This section presents a brief summary of the important outcomes of the research carried out into the design of the high efficiency class-F PA and AIA.

For the nonlinear model of the active device, a novel application of the load/source-pull method has been developed to obtain optimum load and source impedances at the fundamental frequency and the second and third harmonics. Two new designs for the source and the load harmonic matching networks which realise the required optimum impedances have been proposed. Three PAs were designed and fabricated, one for an operating frequency of 0.9 GHz and two for an operating frequency of 2.45 GHz. There was a good agreement between the simulated and measured results.

A detailed study on an H-shaped patch has been carried out. Mode frequency formulas and a systematic design approach are presented. For the probe feed impedance matching, a new matrix input impedance formula has been derived. Two new explicit computationally efficient coupling impedance formulas for a probe feed rectangular segment were derived to evaluate the elements in the matrix impedance formula.

Two AIA designs using the H-shaped patch antenna were designed and fabricated. The practical results are in close agreement with the simulated results.

In Chapter 3 a novel application of the simulated load/source-pull method to obtain the optimum load and source impedances for two class-F PAs operating at 0.9 GHz and 2.45 GHz is presented. Simulated results show that the load and source second harmonics have a more significant effect on the PAE than do the third harmonics. Also, the results show that the effect of the load and source harmonic impedances on the PAE is more critical at 2.45 GHz than at 0.9 GHz. In the application of the load/source-pull method,

using the approach in this thesis, the load/source impedances can be investigated over a wide range of frequencies.

In Chapter 4 a 0.9 GHz class-F PA with the new proposed network was designed and fabricated. The designed PA achieved a measured PAE of 71.4% which is comparable with the results obtained in other published work.

In Chapter 5 two PA designs using new forms of matching networks were designed to operate at the higher frequency of 2.45 GHz. These class-F PA circuits achieved a high efficiency of more than 70% and good agreement between the simulated and measured results is obtained. Again the PAE obtained in this work is comparable to the results reported in other published work.

In Chapter 7 the use of coplanar circuit analysis in the derivation of interport coupling impedances involving the Green's function is described. By using the partitioned form of Green's function and the introduction of closed forms of infinite series new explicit computationally efficient probe feed coupling impedance formulas for a rectangular patch antenna are derived.

In Chapter 8 a new and simpler formula for the fourth mode frequency is derived. A systematic design strategy which reduces the trial and error time for determining the dimensions of the H-shaped patch for a given operating frequency is presented. Applying the new analytic technique of cojoining matrix circuit equations the number of coplanar circuit equations is reduced and simplifies the multiport analysis used to obtain a new explicit matrix input impedance formula for a probe feed H-shaped patch antenna. Two H-shaped patch antennas operating at 2.45 GHz were fabricated. The predicted and simulated values of mode frequencies, input impedances and return losses show good agreement with the measured results.

In Chapter 9 two AIA circuits using the H-shaped patch antenna were investigated. Both designs included the source and load harmonic matching capability which is desired

for high efficiency performance. These AIA circuits achieved a measured PAE of over 65%.

The key requirement in the design of transmitters is to reduce the cost, power consumption, weight and the size. The results of this research carried out will significantly improve the performances of wireless systems (handheld devices and base stations) and hence will be of interest to the commercial market.

10.2 Further Work

In this section three areas of further work are proposed. The first suggestion is to investigate how the efficiency can be improved without sacrificing the stability of the PA. The second proposed area of further work is to improve the PA efficiency over a wide bandwidth by re-designing the load/source matching network and drain/gate bias networks. Thirdly it would be useful to investigate how a U-slot rectangular antenna and a slot-coupled antenna could be used to obtain broadband, and, harmonic suppression in a practical AIA.

10.2.1 Investigation on the trade-off between stability and efficiency of a PA

One of the main causes of power loss in the PA is due to stabilising resistors placed at the gate of the FET which ensure that the FET is stable over the required frequency range. Simulations have shown that by removing the stabilising resistors in the PA circuits presented in Chapter 5 a PAE increase of between 6% and 10% is obtained. Consequently, further research should investigate the trade-off between stability and efficiency. Also an examination of how stability can still be obtained if lower values of resistors are used. The other source of power loss is in the load/source harmonic matching networks realised using

microstrip lines. To reduce these losses the matching networks should be designed to use fewer and shorter lines fabricated on low loss substrates.

10.2.2 Investigation on increasing the PA efficiency over a wide bandwidth

Another important area of research is to increase the PA efficiency over a wide bandwidth. For this the load/source matching networks and the gate/drain bias networks can be re-designed to balance the bandwidth with the PAE over a wide frequency range. This broadband objective is complicated as both the source and load networks must be designed to produce optimum impedances at the fundamental frequency, and second and third harmonics over a wide frequency range. In one approach a photonic band gap (PBG) material is used in the output circuit [147]. Also in [65], [148] a non resonant distributed circuit network is used.

10.2.3 Investigation and design of broadband, harmonic suppressed microstrip patch antennas for AIA design

In broadband AIA design, the antenna must have a broad bandwidth response. Hence an area of further work is to investigate the design of broadband antennas with a harmonic suppression capability. Two approaches are normally used to increase the bandwidth of the antenna. One approach is to use a thick substrate and design the antenna so that the proximity mode frequencies are close to each other, hence producing a broadband response. This might be achieved by using a thick substrate H-shaped patch antenna or a thick substrate U-slot rectangular patch antenna. The properties of the latter antenna are discussed below.

10.2.3.1 U-slot rectangular microstrip patch antenna

Many research works have proposed a probe feed U-slot rectangular patch antenna for improving bandwidth [149]-[151]. The structure of a single-layer U-slot rectangular antenna with a centre probe feed is shown in Figure 10.1.

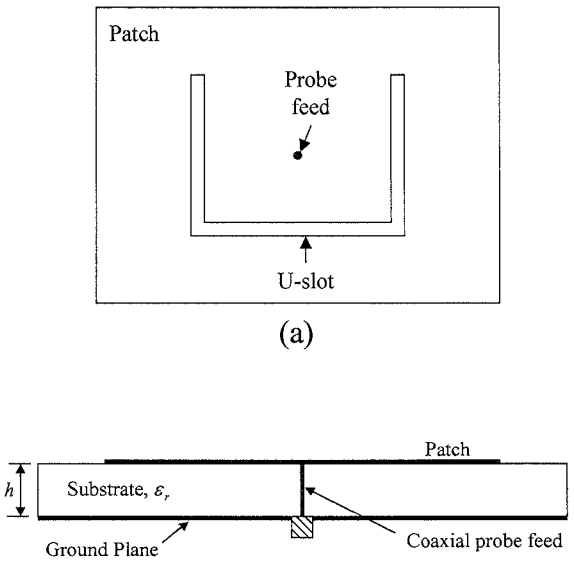


Figure 10.1: Structure of a probe feed U-slot rectangular patch. (a) Top view. (b) Side view.

In [152] the dimensions of a probe feed U-slot rectangular patch with an edge deleted rectangular segment were optimised to achieve harmonic suppression and impedance matching. However the deleted segment resulted in a reduced bandwidth.

In the present research preliminary studies have shown that, for two different substrate thicknesses, a U-slot rectangular antenna can be designed to suppress the second and third harmonics. Most importantly, the second harmonic showed a purely reactive impedance, which would allow the drain bias network to be used to obtain the required optimum second harmonic impedance for high efficiency performance. The bandwidth of the antenna can be further increased by using a low dielectric constant substrate such as air or foam ($\epsilon_r \approx 1$).

10.2.3.2 Slot-coupled microstrip patch antenna

Another approach is to independently optimise the radiating element and the feed network of the antenna. However, to produce a broadband antenna a thick substrate with a low dielectric constant should be used, while, in order to reduce spurious radiation in the feed network a thin substrate with a high dielectric constant should be used. Both opposing requirements can be achieved by using a slot-coupled patch antenna which is discussed briefly in this section.

The structure of a slot-coupled antenna with a microstrip feed line is shown in Figure 10.2, where the signal from the feed network excites the patch antenna through a slot in the ground plane. Consequently, a broadband antenna can be obtained by using a thick substrate with a low dielectric constant such as air and a thin substrate (ϵ_{r2}) with a high dielectric constant to realise a thin microstrip lines and hence reduce spurious radiation.

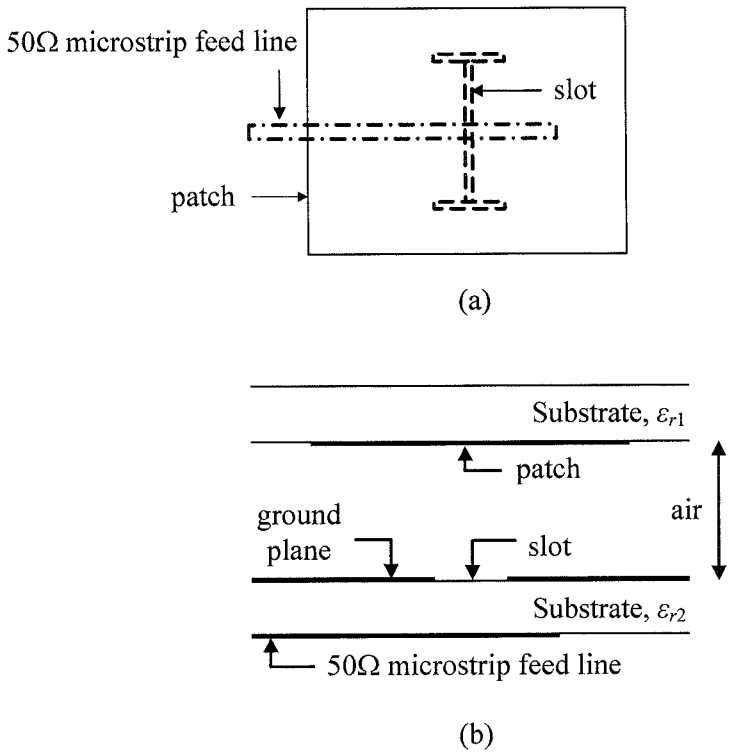


Figure 10.2: Structure of a slot-coupled patch. (a) Top view. (b) Side view.

It is necessary that the locus of the antenna input impedance is close to the required optimum impedance locus in order to obtain maximum efficiency. Further, the mode frequencies of the antenna should not be close to the PA's second and third harmonics. Fortunately the slot-coupled antenna has a number of design parameters which can be deployed to achieve the above objectives. These include the dimensions of the patch, the slot and the open circuit stub. Further two extra tuning stubs can be also used, one on the main feed line and the other on the open circuit stub.

Some initial investigations have already been carried out as reported in [153] where it has been shown that the antenna can suppress the second and third harmonics and obtain the required harmonic load impedances for class-F PA. This antenna structure was designed and modelled using the electromagnetic (EM) simulator and the results obtained agreed with those obtained from practical measurements.

An accurate transmission-line model of this antenna is also required so that the initial performance of the antenna can be quickly obtained using standard library elements (lumped and distributed elements). Then the design can be fine tuned using the EM simulator which gives results more accurately reflecting practical measurement.

A transmission-line model of this antenna has been derived in [115], [154]. However as shown in [115] the equations for the turn ratios of the two transformers (coupling from the feed line to the slot line and coupling from the slot to patch) need to be further investigated to produce more accurate results. Extensive parametric studies can then be carried out (similar to the ones used in the design of the H-shaped antenna) in order to simultaneously obtain a broad bandwidth and harmonic suppression for the antenna.

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APPENDIX 4A Two-Lumped-Element L-C Matching Network Formula

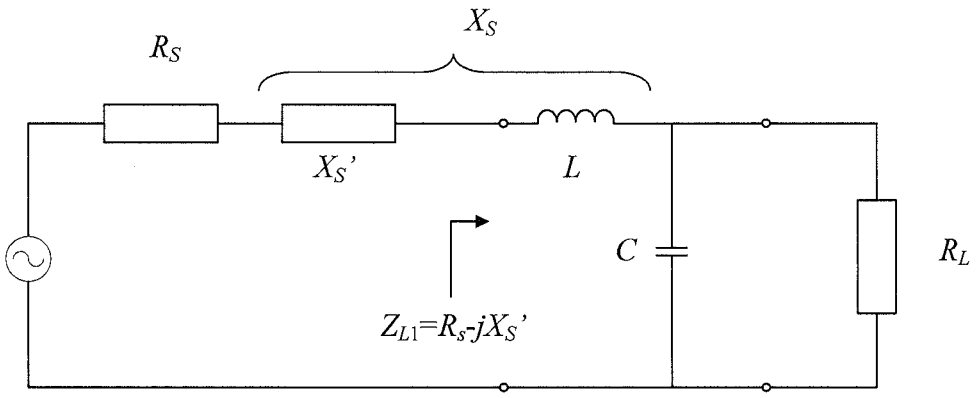


Figure 4A.1: An L-section for matching.

Define : R_S, X_S', R_L, f_1.

Quality-factor, *Q*

$$Q = \sqrt{\frac{R_L}{R_S} - 1} \tag{4A.1}$$

Capacitor value, *C*

$$C = \frac{1}{2\pi f_1 X_p}, \tag{4A.2}$$

where, $X_p = \dfrac{R_L}{Q}$

Inductor value, *L*

$$L = \frac{X_S - X_S'}{2\pi f_1}, \tag{4A.3}$$

where, $X_S = Q\, R_S$

APPENDIX 4B Transformation of Lumped-Elements to Transmission Lines

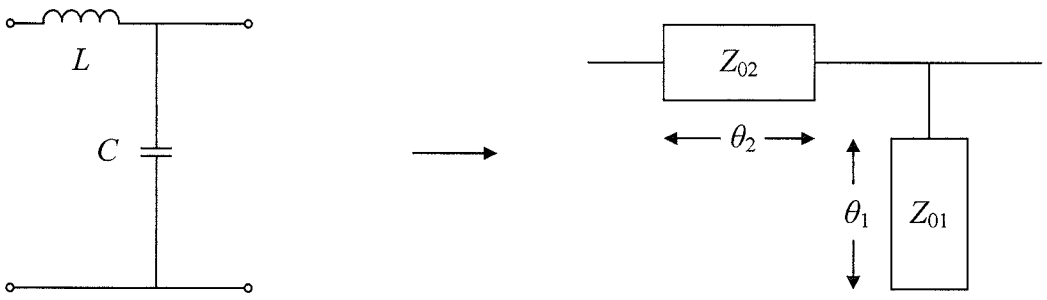


Figure 4B.1: (a) Lumped elements (b) Distributed form (Transmission lines).

Define : C, L, f_1, θ_1 and Z_{02}.

Z_{01}

$$\frac{1}{2\pi f_1 C} = Z_{01} \tan\theta_1 \tag{4B.1}$$

$$Z_{01} = \frac{1}{2\pi f_1 C \tan\theta_1} \tag{4B.2}$$

θ_2

$$2\pi f_1 L = Z_{02} \tan\theta_2 \tag{4B.3}$$

$$\theta_2 = \tan^{-1}\left(\frac{2\pi f_1 L}{Z_{02}}\right) \tag{4B.4}$$

APPENDIX 4C Derivation of the Electrical Length θ_3

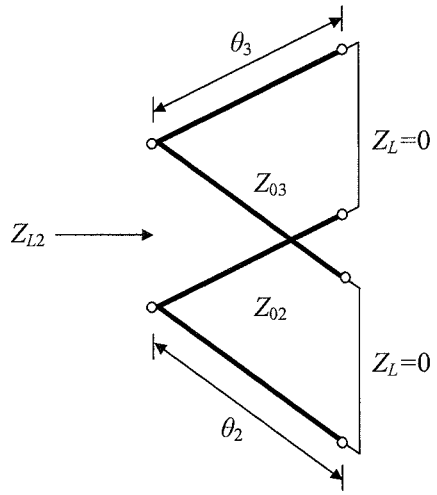


Figure 4C.1: Equivalent circuit for the load second harmonic impedance, Z_{L2}.

Define : Z_{L2}, Z_{02} and θ_2.

θ_3

$$Z_{in} = Z_{in2} \,//\, Z_{in3} = \frac{jZ_{02}\tan 2\theta_2 . jZ_{03}\tan\theta_3}{jZ_{02}\tan 2\theta_2 + jZ_{03}\tan\theta_3}, \tag{4C.1}$$

$$\text{hence}, \theta_3 = \tan^{-1}\left(\frac{1}{Z_{03}}\frac{-Z_{in}Z_{02}\tan 2\theta_2}{Z_{in} - jZ_{02}\tan 2\theta_2}\right). \tag{4C.2}$$

At the second harmonic, $2f_1$

$$\theta_3 = \tan^{-1}\left(\frac{1}{Z_{03}}\frac{Z_{in}Z_{02}\tan 2\theta_2}{jZ_{02}\tan 2\theta_2 - Z_{in}}\right). \tag{4C.3}$$

At the fundamental frequency, f_1

$$\theta_3 = \frac{1}{2}\tan^{-1}\left(\frac{1}{Z_{03}}\frac{Z_{in}Z_{02}\tan 2\theta_2}{jZ_{02}\tan 2\theta_2 - Z_{in}}\right). \tag{4C.4}$$

For $\theta_3 \geq 45°@f_1$,

$$\theta_3 = \frac{1}{2}\left(\pi + \tan^{-1}\left(\frac{1}{Z_{03}}\frac{Z_{in}Z_{02}\tan 2\theta_2}{jZ_{02}\tan 2\theta_2 - Z_{in}}\right)\right). \tag{4C.5}$$

APPENDIX 5A Derivation of the Electrical Length θ_2 and the Characteristic Impedance Z_{02}

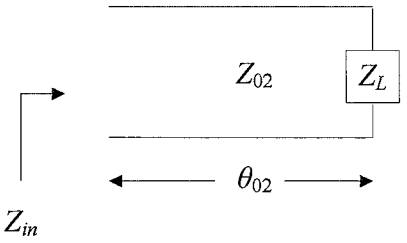


Figure 5A.1: Equivalent circuit for the load fundamental frequency impedance, Z_{L1}.

Define : Z_L, Z_{01}, θ_1, Z_{in}.

The input impedance, Z_{in} in Figure 5A.1 is given by

$$Z_{in} = \frac{Z_{02}(R_L - jX_L + jZ_{02}\tan\theta_2)}{Z_{02} + j(R_L - jX_L)\tan\theta_2} \tag{5A.1}$$

where, Z_L=R_L-jX_L.

Equation (5A.1) multiplied by ($Z_{02} + X_L \tan\theta_2$ - $jR_L \tan\theta_2$) becomes

$$Z_{in} = \frac{Z_{02}\left(R_L Z_{02}\left(1+\tan^2\theta_2\right)+ j\left(Z_{02}\left(Z_{02}\tan\theta_2 + X_L\tan^2\theta_2 - X_L\right)-\left(R_L^{\,2}+X_L^{\,2}\right)\tan\theta_2\right)\right)}{\left(Z_{02}+X_L\tan\theta_2\right)^2+\left(R_L\tan\theta_2\right)^2} \tag{5A.2}$$

where,

$$\mathrm{Re}\{Z_{in}\} = \frac{R_L Z_{02}^{\,2}\left(1+\tan^2\theta_2\right)}{\left(Z_{02}+X_L\tan\theta_2\right)^2+\left(R_L\tan\theta_2\right)^2} \tag{5A.3}$$

and,

$$\mathrm{Im}\{Z_{in}\} = \frac{Z_{02}^{\,2}\left(Z_{02}\tan\theta_2 + X_L\tan^2\theta_2 - X_L\right)- Z_{02}\left(R_L^{\,2}+X_L^{\,2}\right)\tan\theta_2}{\left(Z_{02}+X_L\tan\theta_2\right)^2+\left(R_L\tan\theta_2\right)^2} \tag{5A.4}$$

Values for Z_{02}, θ_2 are obtained by solving the equations (5A.3) and (5A.4).

APPENDIX 5B Derivation of the Electrical Length θ_1

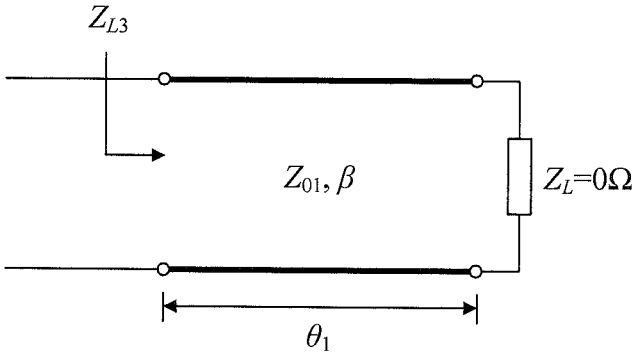


Figure 5B.1: Equivalent circuit for the load third harmonic impedance, Z_{L3}.

Define : Z_{L3} and Z_{01}.

θ_1

$$Z_{L3} = jZ_{01} \tan\theta_1 \tag{5B.1}$$

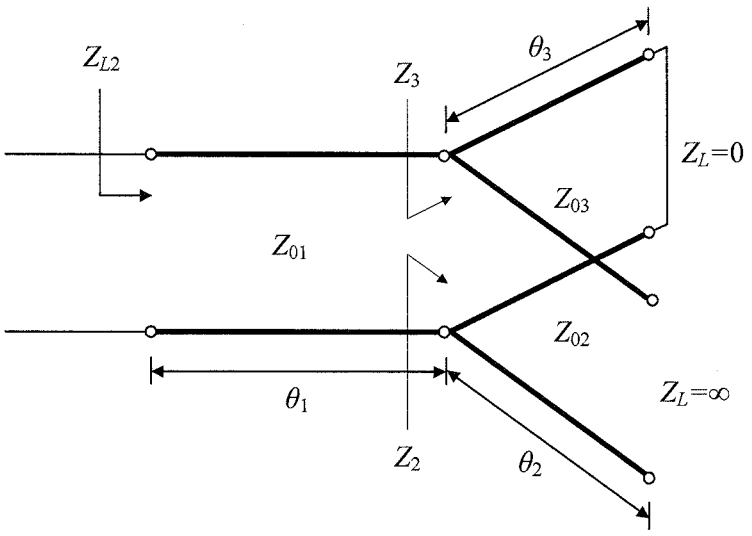
At the 3rd harmonic, $3f_1$

$$\theta_1 = \tan^{-1}\left(\frac{-jZ_{L3}}{Z_{01}}\right) \tag{5B.2}$$

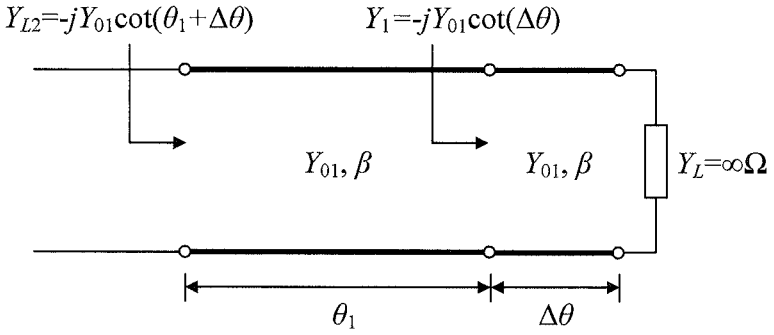
At the fundamental frequency, f_1

$$\theta_1 = \frac{1}{3}\tan^{-1}\left(\frac{-jZ_{L3}}{Z_{01}}\right) \tag{5B.3}$$

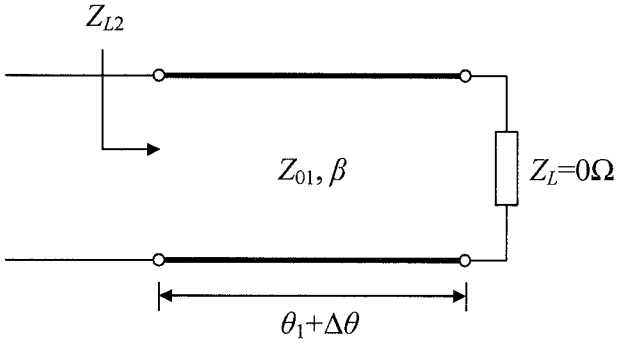
APPENDIX 5C Derivation of the Electrical Length θ_3



(a)



(b)



(c)

Figure 5C.1: Equivalent circuit for the load second harmonic impedance, Z_{L2}.

Define : Z_{L2}, Z_{02}, θ_2 and Z_{03}.

θ_3

$$Y_1 = Y_2 + Y_3 \tag{5C.1}$$

where, $Y_1 = \dfrac{-jY_{01}}{\tan\Delta\theta}$, $Y_2 = jY_{02}\tan\theta_2$, $Y_3 = \dfrac{-jY_{03}}{\tan\theta_3}$.

and hence,

$$\Delta\theta = \tan^{-1}\frac{Y_{01}\tan\theta_3}{Y_{03} - Y_{02}\tan\theta_2\tan\theta_3} = \tan^{-1}\frac{Z_{02}Z_{03}\tan\theta_3}{Z_{01}Z_{02} - Z_{01}Z_{03}\tan\theta_2\tan\theta_3}. \tag{5C.2}$$

$$Z_{L2} = jZ_{01}\tan\left(\theta_1 + \Delta\theta\right) \tag{5C.3}$$

$$Z_{L2} = jZ_{01}\tan\left(\theta_1 + \tan^{-1}\frac{Z_{02}Z_{03}\tan\theta_3}{Z_{01}Z_{02} - Z_{01}Z_{03}\tan\theta_2\tan\theta_3}\right) \tag{5C.4}$$

$$\theta_3 = \tan^{-1}\frac{Z_{01}Z_{02}\tan\left(\tan^{-1}\left(\dfrac{-jZ_{L2}}{Z_{01}}\right) - \theta_1\right)}{Z_{02}Z_{03} + Z_{01}Z_{03}\tan\theta_2\tan\left(\tan^{-1}\left(\dfrac{-jZ_{L2}}{Z_{01}}\right) - \theta_1\right)} \tag{5C.5}$$

At the second harmonic, $2f_1$

$$\theta_3 = \tan^{-1}\left(\frac{Z_{01}Z_{02}}{Z_{03}}\frac{\tan\left(\tan^{-1}\left(\dfrac{-jZ_{L2}}{Z_{01}}\right) - \theta_1\right)}{Z_{02} + 1.732Z_{01}\tan\left(\tan^{-1}\left(\dfrac{-jZ_{L2}}{Z_{01}}\right) - \theta_1\right)}\right) \tag{5C.6}$$

At the fundamental frequency, f_1

$$\theta_3 = \frac{1}{2}\tan^{-1}\left(\frac{Z_{01}Z_{02}}{Z_{03}}\frac{\tan\left(\tan^{-1}\left(\dfrac{-jZ_{L2}}{Z_{01}}\right) - 2\theta_1\right)}{Z_{02} + 1.732Z_{01}\tan\left(\tan^{-1}\left(\dfrac{-jZ_{L2}}{Z_{01}}\right) - 2\theta_1\right)}\right) \tag{5C.7}$$

where, $\tan(\theta_2)$=$\tan(60^o)$=1.732.

APPENDIX 8A Derivation of the First Four Resonant Mode Frequencies of an H-Shaped Microstrip Patch Antenna

As the antenna has symmetric four-fold symmetry geometry, the formulas for the four mode frequencies can be obtained by determining the current path length in a quarter of the antenna geometry, as shown below.

Define : c_0, ϵ_{reff1}, ϵ_{reff2}, ϵ_{reff3}, h, Z_1, Z_2, Z_3, L_1, L_2, W_a, W_1, W_2

f_1

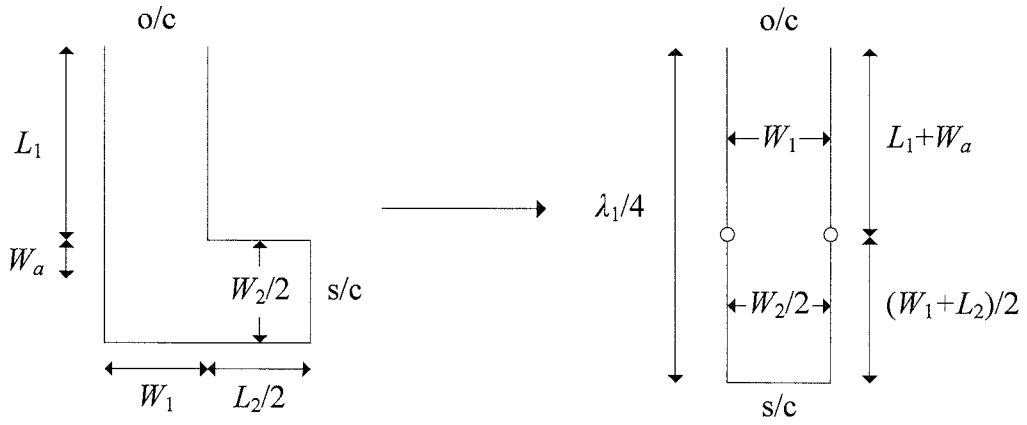


Figure 8A.1: Equivalent microstrip line circuit for mode f_1.

For the first mode frequency, $L_1 + W_a + \frac{W_1}{2} + \frac{L_2}{2} = \frac{\lambda_1}{4}$.

Since $f = \frac{c_0}{\lambda\sqrt{\varepsilon_{reff}}}$ (8A.1)

hence, $f_1 = \frac{c_0}{4(L_1 + W_a)\sqrt{\varepsilon_{reff1}} + 2(W_1 + L_2)\sqrt{\varepsilon_{reff2}}}$. (8A.2)

f_2

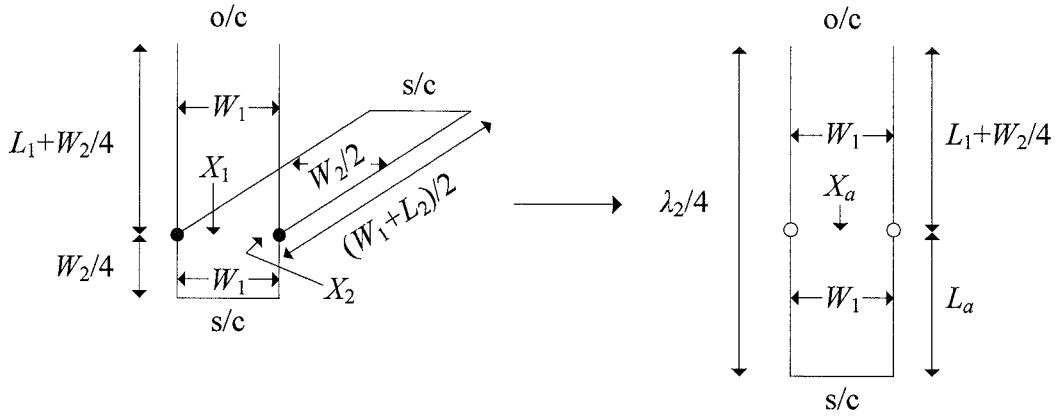


Figure 8A.2: Equivalent microstrip line circuit for mode f_2.

For the second mode frequency, $L_1 + W_2/4 + L_a = \lambda_2/4$, then, f_2 is given by

$$f_2 = \frac{c_0}{(4L_1 + W_2 + 4L_a)\sqrt{\varepsilon_{reff1}}}. \tag{8A.3}$$

The effective length L_a with the width W_1, was obtained by taking into account the two parallel short circuit microstrip lines of length $(W_1+L_2)/2$, and, width $W_2/2$, and, of length $W_2/4$, and, width W_1 as shown below.

Let,

$$X_1 = Z_1 \tan\theta_1 \approx Z_1\theta_1 \approx Z_1 \frac{W_2}{4} k_1, \qquad X_2 = Z_2 \tan\theta_2 \approx Z_2\theta_2 \approx Z_2 \frac{W_1 + L_2}{2} k_2 \qquad \text{and}$$

$$X_a = Z_1 \tan\theta_a \approx Z_1\theta_a \approx Z_1 L_a k_1$$

where, $\theta = kL$, L is the physical length, $k_1 = \frac{2\pi}{\lambda_1}$, $k_2 = \frac{2\pi}{\lambda_2}$ and $\lambda = \frac{c_0}{f\sqrt{\varepsilon_{reff}}}$.

$$X_a = X_1 // X_2, \tag{8A.4}$$

$$\text{so that, } L_a = \frac{1}{2} \frac{Z_2 W_2 (W_1 + L_2)}{Z_1 W_2 \sqrt{\frac{\varepsilon_{reff1}}{\varepsilon_{reff2}}} + 2Z_2(W_1 + L_2)}. \tag{8A.5}$$

f_3

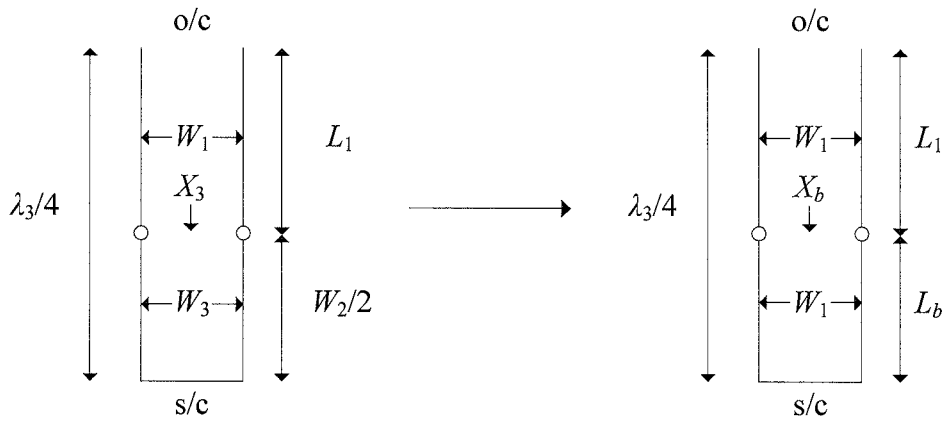


Figure 8A.3: Equivalent microstrip line circuit for mode f_3.

For the third mode frequency, $L_1 + L_b = \lambda_3 / 4$, then, f_3 is given by

$$f_3 = \frac{c_0}{(4L_1 + 4L_b)\sqrt{\varepsilon_{reff1}}}. \tag{8A.6}$$

The effective length L_b with the width of W_1, was obtained by taking into account the short circuit microstrip line of length $W_2/2$, and, width W_3 as shown below.

Let,

$$X_3 \approx Z_3\theta_3 \approx Z_3 \frac{W_2}{2} k_3 \text{ and } X_b \approx Z_1\theta_b \approx Z_1 L_b k_1$$

where, $k_3 = \frac{2\pi}{\lambda_3}$.

$$X_b = X_3, \tag{8A.7}$$

so that, $L_b = \frac{Z_3}{Z_1}\frac{W_2}{2}\sqrt{\frac{\varepsilon_{reff3}}{\varepsilon_{reff1}}}$. (8A.8)

f_4

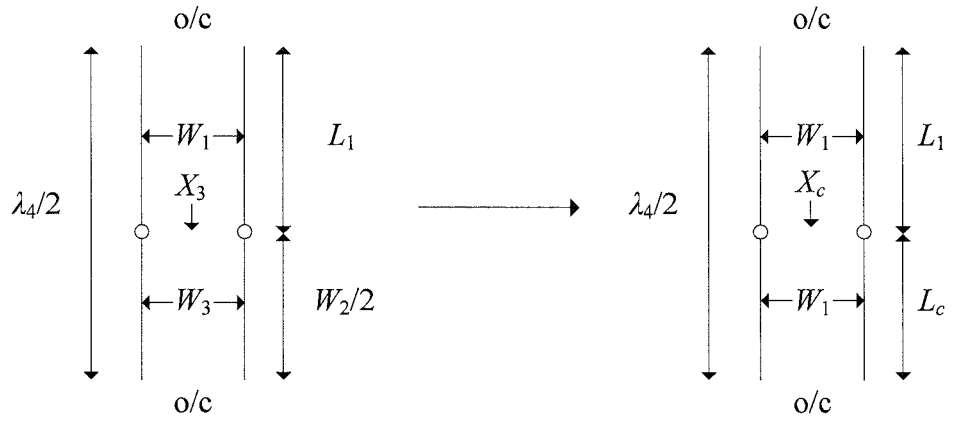


Figure 8A.4: Equivalent microstrip line circuit for mode f_4.

For the fourth mode frequency, $L_1 + L_c = \lambda_4 / 2$, so that, f_4 is given by

$$f_4 = \frac{c_0}{(2L_1 + 2L_c)\sqrt{\varepsilon_{reff1}}}. \tag{8A.9}$$

The effective length L_c with the width of W_1, was obtained by taking into account the open circuit microstrip line of length $W_2/2$, and, width W_3 as shown below.

Let,

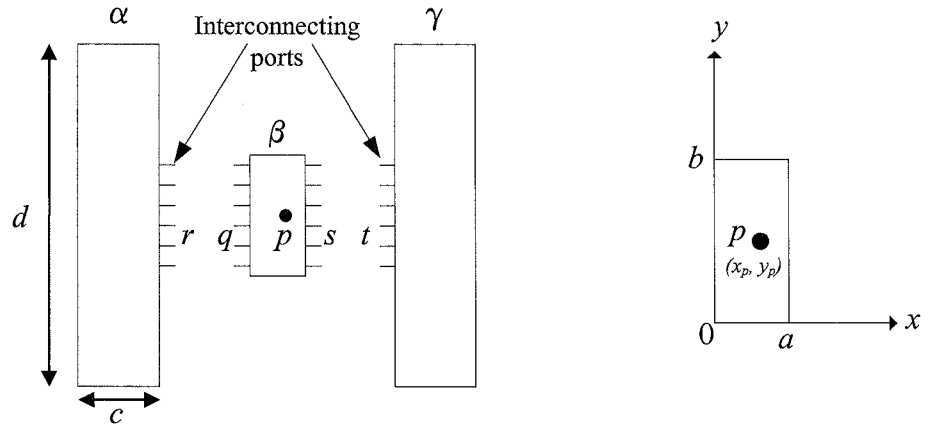
$$X_3 \approx \frac{-Z_3}{\theta_3} \approx \frac{-Z_3}{k_3(W_2/2)} \text{ and } X_c \approx \frac{-Z_1}{\theta_c} \approx \frac{-Z_1}{k_1 L_c}$$

$$X_c = X_3, \tag{8A.10}$$

$$\text{so that, } L_c = \frac{Z_1}{Z_3}\frac{W_2}{2}\sqrt{\frac{\varepsilon_{reff3}}{\varepsilon_{reff1}}}. \tag{8A.11}$$

APPENDIX 8B The MathCAD Program Listing for the Impedance of an H-Shaped Microstrip Patch Antenna

The segmental structure of an H-shaped patch with a probe feed is shown in Figures 8B.1(a) and (b).



(a) (b)

Figure 8B.1: H-shaped microstrip patch antenna (a) Segmental structure (b) β-segment.

Define : $f, \omega, Q, c_0, \varepsilon_0, \varepsilon_r, \varepsilon_{reff}, \mu_0, \mu_r, \mu, k$ (effective wavenumber)

: The dimensions, $h, a, b, c, d, x_p, y_p, W_p, W_q, W_r, W_s$

: M (the upper limit of summation terms)

: N (port number)

Note : The H-shaped patch antenna is symmetric, so segment $\alpha \Leftrightarrow \gamma$.

For Z_{pp} :

Let,

$$B_1 := \frac{b \cdot k}{\pi} \qquad \theta_1 := \frac{\pi}{b}\left(y_p + \frac{W_p}{2}\right) \qquad \theta_2 := \frac{\pi}{b}\left(y_p - \frac{W_p}{2}\right)$$

$$G := \cosh\left(\frac{a \cdot \pi}{b} \cdot \sqrt{n^2 - B_1^{\,2}}\right) + \cosh\left[\frac{(a - 2 \cdot x_p) \cdot \pi}{b} \cdot \sqrt{n^2 - B_1^{\,2}}\right]$$

$$Z_{pp} := 1i \cdot \omega \cdot \mu \cdot h \cdot \left[-\frac{\cos(a \cdot k) + \cos\left[k \cdot (a - 2 \cdot x_p)\right]}{2 \cdot b \; k \cdot \sin(a \cdot k)} \ldots \right.$$
$$\left. + \frac{b^2}{W_p^{\,2} \cdot \pi^3} \cdot \sum_{n=1}^{M} \frac{\left(\sin(n \cdot \theta_1) - \sin(n \cdot \theta_2)\right)^2 \cdot G}{n^2 \cdot \sqrt{n^2 - B_1^{\,2}} \cdot \sinh\left(\frac{a \cdot \pi}{b} \cdot \sqrt{n^2 - B_1^{\,2}}\right)} \right]$$

For Z_{pq} :

Let,

$$L := \frac{\left(\sin(n \cdot \theta_1) - \sin(n \cdot \theta_2)\right) \cdot \left(\sin(n \cdot \theta_3) - \sin(n \cdot \theta_4)\right) \cdot \cosh\left[\frac{(a - x_p) \cdot \pi}{b} \cdot \sqrt{n^2 - B_1^{\,2}}\right]}{n^2 \cdot \sqrt{n^2 - B_1^{\,2}} \cdot \sinh\left(\frac{a \cdot \pi}{b} \cdot \sqrt{n^2 - B_1^{\,2}}\right)}$$

$$Z_{pq} := \left| \begin{array}{l} \text{for } u \in 0 .. N - 1 \\ \quad y_q \leftarrow \dfrac{b \cdot (2 \cdot u + 1)}{2 \cdot N} \\ \quad \theta_3 \leftarrow \dfrac{\pi}{b} \cdot \left(y_q + \dfrac{W_q}{2}\right) \\ \quad \theta_4 \leftarrow \dfrac{\pi}{b} \cdot \left(y_q - \dfrac{W_q}{2}\right) \\ \quad Z_{0,u} \leftarrow 1i \cdot \omega \cdot \mu \cdot h \cdot \left[-\dfrac{\cos\left[k \cdot (a - x_p)\right]}{b \cdot k \cdot \sin(a \cdot k)} + \dfrac{2 \cdot b^2}{W_p \cdot W_q \cdot \pi^3} \cdot \sum_{n=1}^{M} L \right] \\ Z \end{array} \right.$$

For $\boldsymbol{Z}_{ps}$:

Let,

$$P := \frac{\left(\sin\left(n\cdot\theta_1\right) - \sin\left(n\cdot\theta_2\right)\right)\cdot\left(\sin\left(n\cdot\theta_3\right) - \sin\left(n\cdot\theta_4\right)\right)\cdot\cosh\left(\frac{x_p\cdot\pi}{b}\cdot\sqrt{n^2 - B_1^{\,2}}\right)}{n^2\cdot\sqrt{n^2 - B_1^{\,2}}\cdot\sinh\left(\frac{a\cdot\pi}{b}\cdot\sqrt{n^2 - B_1^{\,2}}\right)}$$

$$Z_{ps} := \left| \begin{array}{l} \text{for } u \in 0..N-1 \\ \quad \left| \begin{array}{l} y_s \leftarrow \dfrac{b\cdot(2\cdot u + 1)}{2\cdot N} \\ \theta_3 \leftarrow \dfrac{\pi}{b}\cdot\left(y_s + \dfrac{W_s}{2}\right) \\ \theta_4 \leftarrow \dfrac{\pi}{b}\cdot\left(y_s - \dfrac{W_s}{2}\right) \\ Z_{0,u} \leftarrow 1i\cdot\omega\cdot\mu\cdot h\cdot\left(\dfrac{\cos\left(k\cdot x_p\right)}{b\cdot k\cdot\sin(a\cdot k)} - \dfrac{2\cdot b^2}{W_p\cdot W_s\cdot\pi^3}\cdot\sum_{n=1}^{M} P\right) \end{array} \right. \\ Z \end{array} \right.$$

For $\boldsymbol{Z_{qq}}$:

Let,

$$R := \frac{\left(\sin\left(n\cdot\theta_1\right) - \sin\left(n\cdot\theta_2\right)\right)\cdot\left(\sin\left(n\cdot\theta_3\right) - \sin\left(n\cdot\theta_4\right)\right)\cdot\coth\left(\frac{a\cdot\pi}{b}\cdot\sqrt{n^2 - B_1{}^2}\right)}{n^2\cdot\sqrt{n^2 - B_1{}^2}}$$

$$Z_{qq} := \left|\begin{array}{l} \text{for } u \in 0..N-1 \\ \quad \left|\begin{array}{l} y_q \leftarrow \frac{b\cdot(2\cdot u+1)}{2\cdot N} \\ \theta_1 \leftarrow \frac{\pi}{b}\cdot\left(y_q + \frac{W_q}{2}\right) \\ \theta_2 \leftarrow \frac{\pi}{b}\cdot\left(y_q - \frac{W_q}{2}\right) \\ \text{for } t \in 0..N-1 \\ \quad \left|\begin{array}{l} y_q \leftarrow \frac{b\cdot(2\cdot t+1)}{2\cdot N} \\ \theta_3 \leftarrow \frac{\pi}{b}\cdot\left(y_q + \frac{W_q}{2}\right) \\ \theta_4 \leftarrow \frac{\pi}{b}\cdot\left(y_q - \frac{W_q}{2}\right) \\ Z_{u,t} \leftarrow 1i\cdot\omega\cdot\mu\cdot h\cdot\left(-\frac{\cot(a\cdot k)}{b\cdot k} \ldots + \frac{2\cdot b^2}{W_q{}^2\cdot\pi^3}\cdot\sum_{n=1}^{M} R\right) \\ Z_{t,u} \leftarrow Z_{u,t} \end{array}\right. \\ Z \end{array}\right.$$

For $\boldsymbol{Z_{qs}}$:

Let,

$$S := \frac{\left(\sin\left(n\cdot\theta_1\right) - \sin\left(n\cdot\theta_2\right)\right)\cdot\left(\sin\left(n\cdot\theta_3\right) - \sin\left(n\cdot\theta_4\right)\right)}{n^2\cdot\sqrt{n^2 - B_1^{\,2}}\cdot\sinh\left(\frac{a\cdot\pi}{b}\cdot\sqrt{n^2 - B_1^{\,2}}\right)}$$

$$Z_{qs} := \left|\begin{array}{l} \text{for } u \in 0..N-1 \\ \quad y_q \leftarrow \dfrac{b\cdot(2\cdot u+1)}{2\cdot N} \\ \quad \theta_1 \leftarrow \dfrac{\pi}{b}\cdot\left(y_q + \dfrac{W_q}{2}\right) \\ \quad \theta_2 \leftarrow \dfrac{\pi}{b}\cdot\left(y_q - \dfrac{W_q}{2}\right) \\ \quad \text{for } t \in 0..N-1 \\ \quad\quad y_s \leftarrow \dfrac{b\cdot(2\cdot t+1)}{2\cdot N} \\ \quad\quad \theta_3 \leftarrow \dfrac{\pi}{b}\cdot\left(y_s + \dfrac{W_s}{2}\right) \\ \quad\quad \theta_4 \leftarrow \dfrac{\pi}{b}\cdot\left(y_s - \dfrac{W_s}{2}\right) \\ \quad\quad Z_{u,t} \leftarrow 1i\cdot\omega\cdot\mu\cdot h\cdot\left(\dfrac{1}{b\cdot k\cdot\sin(a\cdot k)} - \dfrac{2\cdot b^2}{W_q\cdot W_s\cdot\pi^3}\cdot\sum_{n=1}^{M} S\right) \\ \quad\quad Z_{t,u} \leftarrow Z_{u,t} \\ Z \end{array}\right.$$

For $\boldsymbol{Z}_{rr}$:

Let,

$$B_2 := \frac{d \cdot k}{\pi}$$

$$T := \frac{\left(\sin\left(n \cdot \theta_1\right) - \sin\left(n \cdot \theta_2\right)\right) \cdot \left(\sin\left(n \cdot \theta_3\right) - \sin\left(n \cdot \theta_4\right)\right) \cdot \coth\left(\frac{c \cdot \pi}{d} \cdot \sqrt{n^2 - B_2^{\,2}}\right)}{n^2 \cdot \sqrt{n^2 - B_2^{\,2}}}$$

$Z_{rr} :=$ for $u \in 0..N-1$

$y_r \leftarrow \frac{b \cdot (2 \cdot u + 1)}{2 \cdot N} + \frac{d - b}{2}$

$\theta_1 \leftarrow \frac{\pi}{d} \cdot \left(y_r + \frac{W_r}{2}\right)$

$\theta_2 \leftarrow \frac{\pi}{d} \cdot \left(y_r - \frac{W_r}{2}\right)$

for $t \in 0..N-1$

$y_r \leftarrow \frac{b \cdot (2 \cdot t + 1)}{2 \cdot N} + \frac{d - b}{2}$

$\theta_3 \leftarrow \frac{\pi}{d} \cdot \left(y_r + \frac{W_r}{2}\right)$

$\theta_4 \leftarrow \frac{\pi}{d} \cdot \left(y_r - \frac{W_r}{2}\right)$

$Z_{u,t} \leftarrow 1i \cdot \omega \cdot \mu \cdot h \cdot \left(-\frac{\cot(c \cdot k)}{d \cdot k} \ldots + \frac{2 \cdot d^2}{W_r^{\,2} \cdot \pi^3} \cdot \sum_{n=1}^{M} T\right)$

$Z_{t,u} \leftarrow Z_{u,t}$

Z

For $\boldsymbol{Z_{in}}$:

$$Z_{in} := Z_{pp} - Z_A \cdot Z_B^{-1} \cdot Z_A^{T}$$

where,

$$Z_A := \text{augment}(Z_{pq}, Z_{ps})$$

$$Z_B := \text{stack}(\text{augment}(Z_{qq} + Z_{rr}, Z_{qs}), \text{augment}(Z_{qs}, Z_{qq} + Z_{rr}))$$

The effective dimensions of the patch were used in the above equations. A run time for a sweep on 501 points of the input impedance for a fixed probe position over the frequency range (2.2 to 2.7 GHz) was about 70 seconds.